UNIVERSITÀ POLITECNICA DELLE MARCHE
FACOLTÀ DI INGEGNERIA

Corso di Laurea Magistrale in Ingegneria Elettronica

STUDIO SULLA FABBRICAZIONE DI OSCILLATORI AD ANELLO UTILIZZANDO MOLECOLE ORGANICHE COME PHENACENE E PERYLENEDICARBOXIMIDE

STUDY ON FABRICATION OF RING OSCILLATORS USING ORGANIC MOLECULES SUCH AS PHENACENE AND PERYLENEDICARBOXIMIDE

Relatore: Chiar.mo
Prof. Claudio Turchetti

Tesi di Laurea di:
Niko Fioravanti

Correlatore: Chiari.mo
Prof. Yoshihiro Kubozono

Anno Accademico 2019 – 2020

Abstract (Italiano)

Questa tesi presenta il lavoro di ricerca svolto su OFET e inverter complementari basati su OFET nel tentativo di affrontare alcuni problemi. L'obiettivo è sviluppare un oscillatore ad anello ad alte prestazioni costituito da inverter complementari a cinque stadi basati su OFET.

In questo lavoro l'obiettivo è la fabbricazione di oscillatori ad anello utilizzando molecole organiche come phenacene e perylendicarboximide. Le molecole di phenacene sono una classe di composti organici costituiti da anelli aromatici fusi. Sono idrocarburi policiclici aromatici, legati ad aceni ed eliceni dai quali si differenziano per la disposizione degli anelli fusi.

In questa tesi di laurea, l'autore descrive il background di questo studio nel capitolo 1. Le condizioni sperimentali per la fabbricazione di dispositivi OFET sono descritte nel capitolo 2. La caratterizzazione delle proprietà FET in questo studio è mostrata nel capitolo 3 ed i dati degli oscillatori ad anello sono presentati nel capitolo 4.

Nel capitolo 3, l'autore descrive le caratteristiche FET degli OFET organici a film sottile. Nella sezione 3.1, sono riportate le proprietà degli OFET a film sottile costituiti da [7]phenacene su substrati di Si, in cui SiO_2 e ZrO_2 sono usati per i dielettrici di gate. Questi dispositivi hanno mostrato caratteristiche FET di tipo *p* normalmente-OFF. Il valore μ più elevato nei FET a film sottile costituiti da [7]phenacene con dielettrico SiO_2 è 1,20 $cm^2 V^{-1} s^{-1}$.

Nella sezione 3.2, l'autore descrive le caratteristiche degli OFET e il comportamento dell'inverter degli inverter CMOS organici realizzati con [7]phenacene come strato attivo per gli OFET a canale *p* e PTCDI-C8 come strato attivo per gli OFET a canale *n*. Gli inverter CMOS organici sono stati fabbricati su diversi substrati come Si, PEN e PET e con diversi dielettrici di gate come SiO_2, ZrO_2 e parylene.

Il valore più alto di guadagno (dV_{out} / dV_{in}) raggiunto è 304, in un substrato PEN spesso 125 μm. Come dielettrico di gate è stato utilizzato parylene spesso 1 μm.

Nel capitolo 4 l'autore descrive le proprietà degli oscillatori ad anello organici realizzato con [6]phenacene e $(C_{14}H_{29})_2$-picene come strato attivo per gli OFET a canale *p* e PTCDI-C8 come strato attivo per gli OFET a canale *n.* Sono stati fabbricati oscillatori ad anello che utilizzano SiO_2 e ZrO_2 come dielettrico di gate per gli OFET. ZrO_2 è stato utilizzato per ottenere il funzionamento a bassa tensione. La frequenza di 25 Hz è stata ottenuta con questo tipo di dispositivo. La migliore prestazione per un oscillatore ad anello organico fabbricato in questo studio è stata di 26 Hz per l'oscillatore ad anello costituito da OFET composti con [6]phenacene (canale *p*) e PTCDI-C8 (canale *n*) come strati attivi e SiO_2 come dielettrico di gate.

Attraverso questo studio, l'autore è riuscito nella fabbricazione di un oscillatore ad anello organico composto da OFET con funzionamento ad alta μ e bassa tensione. Questo studio fornirebbe la base per i futuri dispositivi elettronici pratici/compatibili con l'uomo.

Abstract (English)

This dissertation presents research work performed on OFETs and OFET-based complementary inverters in attempt to address some of issues. The objective is to develop high-performance ring-oscillator consisted of five stage OFET based complementary inverters.

In this work the target is fabrication of ring oscillator using organic molecules such as phenacene and perylenedicarboximide. Phenacenes are a class of organic compounds consisting of fused aromatic rings. They are polycyclic aromatic hydrocarbons, related to acenes and helicenes from which they differ by the arrangement of the fused rings.

In this master thesis, the author describes the background of this study in chapter 1. The experimental conditions for fabrication of OFET devices are described in chapter 2. The characterization of FET properties in this study are shown in chapter 3 and the data of the organic ring oscillator are presented in chapter 4.

In chapter 3, the author describes the FET characteristics of organic thin-film OFETs. In section 3.1, the FET properties of [7]phenacene thin-film OFETs on Si substrates are reported, in which SiO_2 and ZrO_2 are used for gate dielectrics. These devices showed *p*-channel normally-off FET characteristics. The highest μ value in [7]phenacene thin-film FET with SiO_2 dielectric was 1.20 $cm^2 V^{-1} s^{-1}$.

In section 3.2, the author describes the FET characteristics and the inverter behavior of organic CMOS inverters made with [7]phenacene as active layer for *p*-channel OFETs and PTCDI-C8 as active layer for *n*-channel OFETs. Organic CMOS inverters were fabricated on to different substrates such as Si, PEN and PET and with different gate dielectric such as SiO_2, ZrO_2 and parylene.

The highest value of gain (dV_{out}/dV_{in}) reached is 304, in 125 μm thick PEN substrate. In this case 1 μm thick parylene was used as gate dielectric.

In chapter 4 the author describes the properties of organic ring oscillator made with [6]phenacene and $(C_{14}H_{29})_2$-picene as active layer for *p*-channel FETs and

PTCDI-C8 as active layer for *n*-channel FETs. Ring oscillator using SiO_2 and ZrO_2 as gate dielectric for FETs were fabricated. ZrO_2 was used to accomplish low voltage operation. The frequency of 25 Hz was obtained with this type of device. The best performance for an organic ring oscillator fabricated in this study was 26 Hz for ring oscillator made of FETs composed with [6]phenacene (*p*-channel) and PTCDI-C8 (*n*-channel) as active layers and SiO_2 as gate dielectric.

Through this study, the author succeeded in the fabrication of organic ring oscillator composed of OFETs with high μ and low voltage operation. This study would provide the basis for the future practical/human-compatible electronic devices.

Contents

Chapter 1: Organic Field-Effect Transistors

In this chapter the history of FET and CMOS technology is presented. Also, an overview of organic materials and organic devices is given.

Organic materials consist of organic compounds, that is molecules which mainly contain the element carbon (symbol C and atomic number 6). Semiconductors based on organic molecular components are prevalently composed of hydrogen (H), carbon, and oxygen (O).

For organic electronics, of course organic compounds that provide easily displaceable charges are required, which is better satisfied by π-conjugated systems. Organic semiconductors are amorphous or polycrystalline in which the charge transport occurs through hopping of charges between delocalized π molecular orbitals.

1.1 Background

In this section a presentation of the background of FET and CMOS technology is given. The history of the device's development is presented from early XX century.

1.1.1 History of FET

The metal-oxide-semiconductor field-effect transistor (MOSFET), is a type of insulated-gate field-effect transistor (IGFET) that is fabricated by the controlled oxidation of a semiconductor, typically silicon.

In 1925, an Austro-Hungarian physicist, Julius Edgar Lilienfeld, proposed the basic principle of the field-effect transistor (FET) [1] [2], but he was unable to build a working practical semiconducting device based on the concept.

Oskar Heil in the 1930s and William Shockley in the 1940s also theorized the FET operation principle, but they were unsuccessful (Schockley's team built

instead a point-contact transistor, first working transistor, followed by bipolar junction transistor, BJT) [3]. In 1956, Schockley's group won the Nobel prize in Physics for their researches on semiconductors and their discovery of the transistor effect. However, this type of transistor was difficult to manufacture on a mass-production basis, therefore, FETs were theorized as potential alternatives to junction transistors.

The first FET device to be successfully built was the junction field-effect transistor (JFET) by Heinrich Welker and Herbert Francois Mataré in 1945 [4]. Subsequently, M. M. Atalla and D. Kahng at Bell Lab. invented the first successfully operated field-effect transistor (FET) [5] (schematic shown in Figure 1.1).

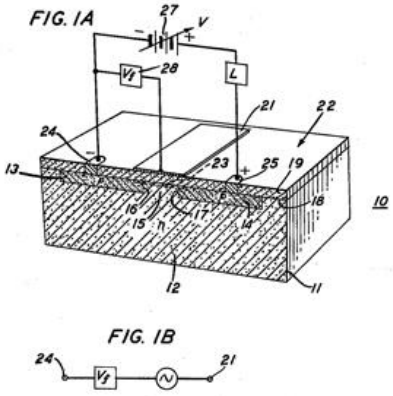


Figure 1.1 *Schematic representation of the first-stage FET device taken from* [5]

They investigated the surface properties of silicon semiconductors, a new method of semiconductor device fabrication was adopted, coating a silicon (Si) wafer with an insulating layer of silicon oxide (SiO_2), so that electricity could reliably penetrate to the conducting silicon below, overcoming the surface states that prevented electricity from reaching the semiconducting layer. This is known as surface passivation [6]. They fabricated the device in November 1959 and presented it as the "silicon–silicon dioxide field induced surface device" in early

1960. A memorandum written by Kahng [7] pointed out a potential application of the MOSFET for integrated circuits and an ease of its fabrication.

Despite the breakthrough, the MOSFET was initially overlooked and ignored by Bell Labs in favour of bipolar transistors. However, engineers of some companies such as Fairchild Semiconductor and Radio Corporation of America (RCA) recognized the advantages of MOSFET at that time. Chih-Tang Sah at Fairchild in late 1960 began building an MOS-controlled tetrode, which he presented in 1961 [8]. In 1963, the first formal public announcement of the MOSFET's existence as a potential technology was made and, in 1964, the device was commercialized. The early MOSFETs commercialized by General Microelectronics and Fairchild were *p*-channel (PMOS) devices for logic and switching applications.

1.1.2 History of CMOS technology

Complementary metal-oxide-semiconductor (CMOS) is a type of MOSFET fabrication process. CMOS is also sometimes explained as complementary-symmetry metal-oxide-semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of *p*-type and *n*-type MOSFETs for logic functions. Schematic of a CMOS device is shown in Figure 1.2. Integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips (including CMOS BIOS), and other digital logic circuits take advantage of CMOS technology which is also used for analog circuits such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication.

Previous section presented the history of MOSFET development ad it turned up that Mohamed M. Atalla and D. Kahng invented the MOSFET at Bell Labs in

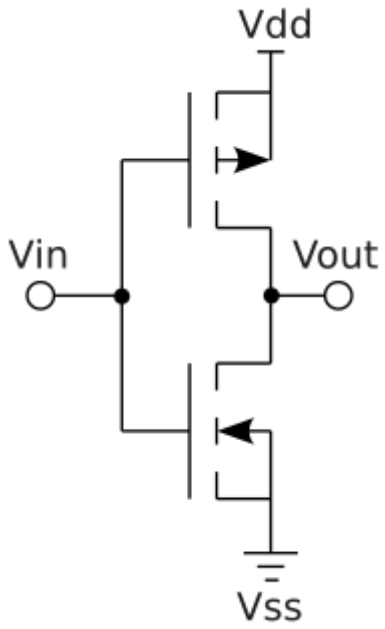


Figure 1.2 *Schematic of a CMOS inverter (NOT logic gate)*

1959, and then demonstrated the transistors fabrication processes in 1960. In 1963 Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor combined and adapted the processes presented by Kahng and Atalla into the CMOS technology [9] [10].

RCA Research Laboratories and the Somerville Manufacturing operation pioneered the production of CMOS technology for very low-power integrated circuits, first in aerospace and later in commercial applications. Gerald Herzog led a major CMOS logic and memory circuit design program for an Air Force computer in 1965 [11]. In 1968 the company demonstrated a 288-bit static RAM and introduced the first members of the popular CD4000 family of general-purpose logic devices [12].

In 1969, Toshiba developed a circuit technology with lower power consumption and faster operating speed than ordinary CMOS. They called it C^2MOS (Clocked CMOS). Toshiba used this novel circuit tecnique to develop a large-scale integration (LSI) chip for a desktop calculator, developed in 1971 and released in 1972 [13].

The first high-volume applications for CMOS circuits emerged in battery-operated consumer products such as digital watches and portable instruments that did not demand the ultimate in speed.

In 1978, Toshiaki Masuhara research team of Hitachi introduced the twin-well Hi-CMOS process, with its HM6147 (4 kb SRAM) memory chip, manufactured with a 3 μm process [14]. This group described a high-speed RAM, the combination of smaller lithography with the silicon-gate process enabled CMOS to compete in performance with bipolar and conventional MOS. In the 1980s, CMOS microprocessors overtook NMOS microprocessors [15].

1.1.3 History of organic FET

Till now, the Si-based technologies and devices are still the main stream. However, with the challenges arising from the considerable miniaturization, further development becomes more and more severe. On the other hand, many new materials and new technologies are emerging, such as nano wire, graphene and organic materials. In fact, the OMs have been studied from 1940s, but due to their poor electrical characteristics (high resistivity, low mobility) and the lack of understanding of transport mechanism during that time, the progress in this domain remained relatively very slow. Though their electron mobility is much lower than that of typical semiconductors, organic semiconductors (OSCs) show promise in low-cost, flexible, lightweight, and environmental-friendly semiconductor applications.

The history of organic electronics started from both the organic FET and organic optoelectronic devices such as light emitting diode (LED). In early 1950s André Bernanose and his group made the first observations of electroluminescence in organic materials [16] [17] [18]. Concerning FETs, in 1986, Mitsubishi Electric researchers H. Koezuka, A. Tsumura and Tsuneya Ando reported the first organic field-effect transistor, based on a polymer

of thiophene molecules [19] [20]. This group fabricated the FET using polythiophene; the field-effect mobility, μ, was ~10^{-5} cm^2 V^{-1} s^{-1}. Then, OFETs using poly (3-hexylthiophene) as an active semiconductor were reported in 1988 [21]. Then, in 1989, Horowitz *et al*. demonstrated the first OFET using a small-molecule semiconductor α-sexithiophene with a higher carrier mobility of 10^{-3} cm^2 V^{-1} s^{-1} and an on/off current ratio of 10^5 [22]. Pentacene, the most important small-molecule semiconductor so far, was applied to OFETs in 1991 and provided *p*-channel operations [23] [24].

In 1996, Z. Bao *et al.* fabricated the FET using polythienylenevinylene, which exhibited the μ value as high as 0.22 cm^2 V^{-1} s^{-1} [25]. From early XXI century, organic field effect transistors (OFETs) have been increasingly present as a research object. Both, academy and industry, have made many steps forward in the past two decades, in order to boost organic electronics into commercial market. This attention is due to their good workability of the solution, low temperature deposition, low cost and compatibility with printing technology on large areas. Differently from the the thin-film deposition of conventional semiconductor that usually needs high temperature process and dustless conditions which significantly increase the fabricating cost.

OFETs can be used in applications such as active matrix displays, radio frequency identification tags, image sensing and they are well suited to switches and amplify mechanical actuations. They are also suitable to integrate logic circuitry and memory arrays into low-cost electronic products such as smart cards, smart price and inventory tags, and large-area sensor arrays.

Their hole mobility was found to be comparable to that of amorphous silicon (a-Si), with values exceeding 1.0 cm^2 V^{-1} s^{-1} [26]. Thus, the FET properties have been improved since the beginning of 2000s. Currently, the organic FET exhibiting the highest μ value is realized using a single crystal of *κ*-(BEDT-TTF)$_2$Cu[N(CN)$_2$]Br (BEDT-TTF: bis(ethylenedithio)tetrathiafulvalene) [27], in which μ reaches 94 cm^2 V^{-1} s^{-1}. In case of thin film, the highest μ value (= 21

$cm^2\ V^{-1}\ s^{-1}$) is achieved in a 3,10-ditetradecylpicene ($(C_{14}H_{29})_2$-picene) thin-film FET with $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) gate dielectric [28].

Moreover, thin-film and single-crystal FETs have been fabricated using more extended phenacene molecules than picene [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40]. Among them, the μ value of [6]phenacene thin-film FET reached 7.4 $cm^2\ V^{-1}\ s^{-1}$ which is one of the highest μ values in organic thin-film FETs. A μ value as high as 18 $cm^2\ V^{-1}\ s^{-1}$ has been recorded in [9]phenacene single-crystal FETs with ZrO_2 gate dielectric. A thin-film FET using alkyl-substituted picene (3,10-ditetradecylpicene: (C14H29)2-picene) provided a μ value as high as 20.9 $cm^2\ V^{-1}\ s^{-1}$, which was one of the best μ values recorded in a two-terminal measurement mode. Therefore, phenacene molecules are promising materials for high-performance FET devices.

Quite different from inorganic counterparts, organic semiconducting molecules are packing up through van der Waals forces and π–π interactions rather than rigid covalent bonds. The weak intermolecular interaction not only makes organic semiconductors potentially soluble and easy to be processed in solution, but also endows organic electronic devices the nature of flexibility.

Previous demonstrations of organic complementary circuits often show high operating voltage, small noise margins, low dc gain, and electrical instability such as hysteresis and threshold voltage shifts. There are two obstacles to developing organic complementary circuits: the lack of high-performance *n*-channel OFET devices, and the processing difficulty of integrating both *n*- and *p*-channel organic field-effect transistors (OFETs) on the same substrate.

1.1.4 History of organic CMOS circuits

Practical organic electronic devices should be realized with a complementary device architecture (utilizing both positive and negative gate bias to turn transistors on and off). In 1996, A. Dodabalapur research team reported the very

first complementary organic circuits [41]. In 1999, at Bell Laboratories., Y. Y. Lin and A. Dodabalapur presented a ring oscillator based on complementary inverters [42]. In the next two years, B. Crone, Lin and Dodabalapur demonstrated the design and fabrication of large-scale complementary integrated circuits based on organic transistors [43] [44]. After these works at Bell Labs., other research teams reported more organic complementary inverters based on different materials, using similar methods with a gain higher than 10 and an output voltage swing close to the supply voltage [45] [46] [47] [48]. However, the mentioned inverter required supply voltage (V_{DD}) higher than 40 V. This is mostly due to the high threshold voltage and low mobility of *n*-channel OFETs. Therefore, these circuits weren't suitable for practical applications.

The development of thin gate dielectrics has made low-voltage operation possible for organic complementary circuits [49] [50]. In particular, Klauk demonstrated ultra-low power consumption complementary circuits operating between 1.5 and 3.0 V using ultra-thin Al_2O_3 treated with a self-assembled monolayer (SAM) as gate dielectrics. Also, other structures such as a double-gate structure (top-gate and bottom-gate) [51], and patterned *n*- and *p*-type semiconductors by means of integrated shadow masks [52] has been tested.

However, *n*-channel OFETs often show inferior performance compared to their counterparts (pentacene *p*-channel OFETs) with a mobility more than one order of magnitude lower. Complementary inverters with comparable mobilities and threshold voltages were reported using pentacene *p*-channel OFETs and C_{60} *n*-channel OFETs. With matched performance in both transistors, the switching voltage of the inverter can be as low as 1.5 V with a dc gain as high as 150 [53]. However, the inverter showed a large hysteresis in the transfer characteristics indicating high trapping density at the dielectrics, which induces electrical instability upon operation.

Concerning the study of organic ring oscillators, the first devices were fabricated in late 90'. In 1997, Brown *et al.* presented a ring oscillator made of metal-insulator-semiconductor field-effect transistors using conjugated organic

semiconductors which gave an oscillation frequency equal to 2 KHz [54]. Ring oscillators composed of *n* stage of CMOS inverter have been fabricated during the last two decades with oscillation frequency exceeding 1 MHz [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73].

Organic ring oscillator made of phenacene molecules has been fabricated by Kubozono's team. This type of ring oscillator shows poor operation with oscillation frequency of 1 Hz [74].

1.2 OFETs characterization

The operation mode of OFETs can be described, to first approximation, by the standard MOSFET models. The device consists of a conductor called the gate (made of metal or a highly doped semiconductor) an insulating layer (which we will call the oxide layer, as an inheritance from silicon technology) of thickness d_{ox} (resulting in capacitance density $C_{ox} = \varepsilon_{ox}/d_{ox}$, with ε_{ox} the permittivity of the insulator material) and a substrate in which the channel will form (Fig. 1.3). This section explains briefly the standard MOSFET regimes and subsequently the operation mode of OFETs.

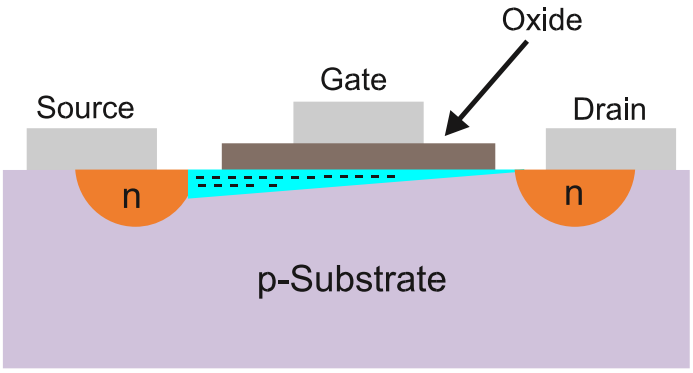


***Figure* 1.3.** *Schematic representation of a n-channel-MOSFET device. The semiconductor bulk is p-doped. The orange areas represent the source-drain electrodes obtained by doping. The blue area is the conduction channel and the signs (-) represent the electrons injected by the source/drain electrode in the presence of a traversal electrical field due to a source-drain voltage $V_{DS} > 0$ applied.*

1.2.1 Standard MOSFET model

A MOSFET is an electronic device, which enables the control of the charge carriers via the application of an electric field at the MOS capacitor. The charges are injected and collected by the source and drain electrodes, respectively. As an example, Figure 1.3 presents a *n*-channel MOSFET device as it is used in silicon (Si) or germanium (Ge) semiconductors. The metal is deposited on the source-drain electrodes and on the oxide layer. The FET device can be categorized to either *n*-channel FET or *p*-channel FET, depending on the type of carrier. An intrinsic semiconductor can be changed to *n*-type or *p*-type extrinsic semiconductor by doping with some electron donors or acceptors, and the extrinsic semiconductors are utilized for the MOSFET. The element-doped Si is commonly used for the active layer of MOSFET. When intrinsic Si is doped with an electron donor, the Si becomes *n*-type Si. When it is doped with an electron acceptor, the Si becomes *p*-type Si. The doping elements belong to group III or V. If an *n*-type semiconductor, where the majority carriers are electrons, is used for MOSFET, the MOSFET generally operates in *p*-channel. On the other hand, if a *p*-type semiconductor, where a majority carrier is hole, is employed for MOSFET, the MOSFET generally operates in *n*-channel. Referring to Figure 1.3: at source and drain, it allows the electrical contact to the channel, defined in the semiconductor substrate via *p*-type doping. The same substrate, but *n*-type doped, is used as source and drain electrode underneath their metallic leads. A gate bias voltage (V_G) applied to the gate contact generates an electric field in the dielectric material, which regulates the source-drain current by modifying the charge carrier density in the channel.

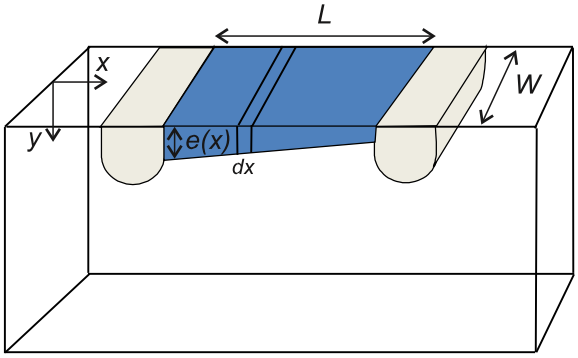


***Figure* 1.4.** *Schematic representation of a MOSFET device employed for approximations leading to the determination of the source-drain current expression.*

A description of the source-drain current flowing in the conduction pathway is typically obtained on the base of several assumptions: (1) interface states and fixed oxide charge or work function difference are resumed in the threshold voltage V_T; (2) the electric current is only induced by an electric field (drift current); (3) the charge carrier mobility is constant in the conduction channel; (4) the doping is uniform along the channel; (5) the leakage current is negligible; (6) the vertical electrical field E_y is much larger than the longitudinal electric field E_x. The last assumption is the so-called gradual approximation.

The density of charges ρ inside the channel varies from one electrode (source, $x = 0$) to the other (drain, $x = L$). To calculate the currents through the device, we have to understand that, locally, the current $I(x)$ at a given point x in the channel is equal to the local induced charge, multiplied by the carrier mobility μ, the field felt by the charges, and the channel width W.

The charge Q flowing through a minimal segment dx of n-channel MOSFET with a channel width W and a channel thickness $e(x)$ (Figure 1.4) is given by:

$$Q = -C_{ox}(V_{GS} - V_{TH} - V(x)) \quad \text{with} \quad V_{TH} = \pm\frac{qn_0e(x)}{C_{ox}} + V_{fb} \qquad (1.1)$$

Where C_{ox} is the MOS capacitor, V_{GS} the gate bias, $V(x)$ the source-drain voltage, q the elementary charge, n_0 free charge density at equilibrium and V_{fb} the flatband potential.

The channel resistance of a minimal segment dx is given as following:

$$dR = \frac{dx}{W\mu|Q|} \tag{1.2}$$

The voltage drop across this minimal segment is defined as following:

$$dV = I_{DS}dR = \frac{I_{DS}dx}{W\mu|Q|} \tag{1.3}$$

Where I_{DS} is the source-drain current and is constant along the conduction channel. By using equations (1.1) and (1.3) and integrating from source ($x = 0$ and $V = 0$) to drain ($x = L$ and $V = V_{DS}$) we obtain the following operation:

$$I_{DS}\int_0^L dx = \int_0^{V_{DS}} -\mu C_{ox} W(V_{GS} - V_{TH} - V(x))dV \tag{1.4}$$

The resolution of this operation yields the following equation:

$$I_{DS} = \frac{W\mu C_{ox}}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{1.5}$$

Depending on V_{DS} and V_{GS} three regimes of current are identified as follows:

Cut-off regime. When $V_{GS} \leq V_{TH}$ the channel is not formed therefore, $I_{DS} = 0$.

Linear regime. Here, $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{GS} - V_{T,}$ the source-drain current has the form:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1.6)$$

Saturation Regime. In this case, $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_T$ and the channel is blocked. In this way, the charge and voltage distribution across the device (except for an infinitely thin zone) is independent of the drain–source voltage and hence the current is constant. The source-drain current is obtained by following approximation:

$$V_{DS} = V_{GS} - V_{TH} \quad (1.7)$$

and its expression is defined as:

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (1.8)$$

1.2.2 Architecture of OFETs

OFETs have different structure and geometries. They can be configured into four basic structures, based on position of the electrodes (Fig. 1.5). OFETs can be grouped in two categories according to the position of the gate electrode. The bottom gate transistors that are again subdivided according to the position of the contact. The patterned source/drain electrodes can be deposited prior to the organic semiconductor (OSC) deposition or after it. The former case is a "coplanar"' configuration (popularly called bottom contact) and the latter is "staggered" configuration (also known as top contact). In these structures, the insulator film is located at the bottom of the semiconductor film. The second category is the top gate transistors and they are, like the first case, subdivided according to the position of the contacts: *top gate, top contact* and *top gate,*

bottom contact transistor. Here the dielectric material is deposited on top of the semiconductor film.

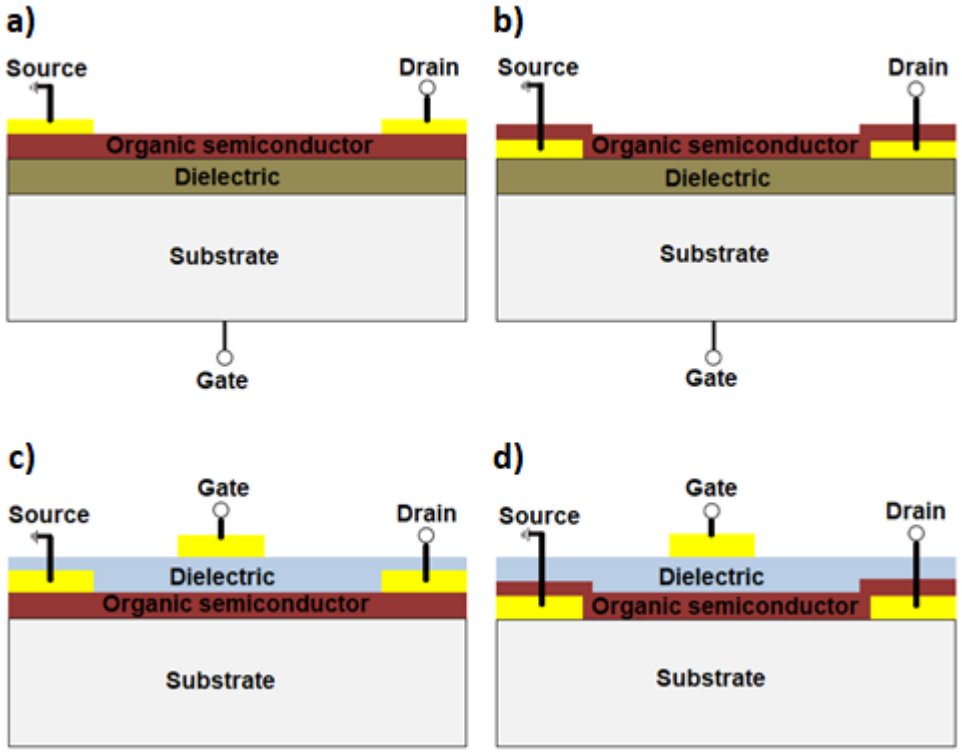


Figure 1.5 *Geometries of organic FET: a) bottom gate, top contact if the electrodes are deposited on top of the semiconductor layer; b) bottom gate, bottom contact if the semiconductor film is deposited on top of the electrode materials; c) top gate, top contact if the source-drain electrodes material are deposited on top of the conductive film; d) top gate, bottom contact if the semiconductor film is deposited on top of the source-drain electrodes.*

1.2.3 OFET Devices

The standard MOSFET models provide a scheme in which the different regimes of the source-drain current can be characterized. These regimes are the linear and the saturation regimes. Figure 1.6 shows the transfer and the output characteristics obtained in one of the OFET devices presented in this thesis.

From this figure, a linear regime is observed for source-drain voltages $V_{DS} < 5$ V and a saturation regime at high V_{DS} is also depicted. The operation mode of both OFET and MOSFET devices are conceptually different: whereas the MOSFET

device works in inversion mode, an OFET operates in accumulation mode. Accumulation means that the application of the gate voltage generates an electric field in the dielectric, which accumulates majority charges of the semiconductor film at the insulator/semiconductor interface, that serves then as conductive channel. Consequently, charge carriers that are injected from source-drain electrode can flow across the channel. Figure 1.7 shows the band structure at the insulator/semiconductor interface, when an electric field is created in the dielectric film by a gate bias. For a *p*-type semiconductor, holes accumulate at the interface, when a negative gate bias is applied (Figure 1.7b). A positive gate bias, however, further suppresses the density of charge carriers in the channel, this regime is called depletion (Figure 1.7c). When choosing, in contrast, *n*-type semiconductors, Figure 1.7d and Figure 1.7e depict the accumulation and the depletion at the interface by a positive and a negative gate bias. Further, at the absence of a gate voltage, the charge carriers at the interface are only thermally generated (Figure 1.7a).

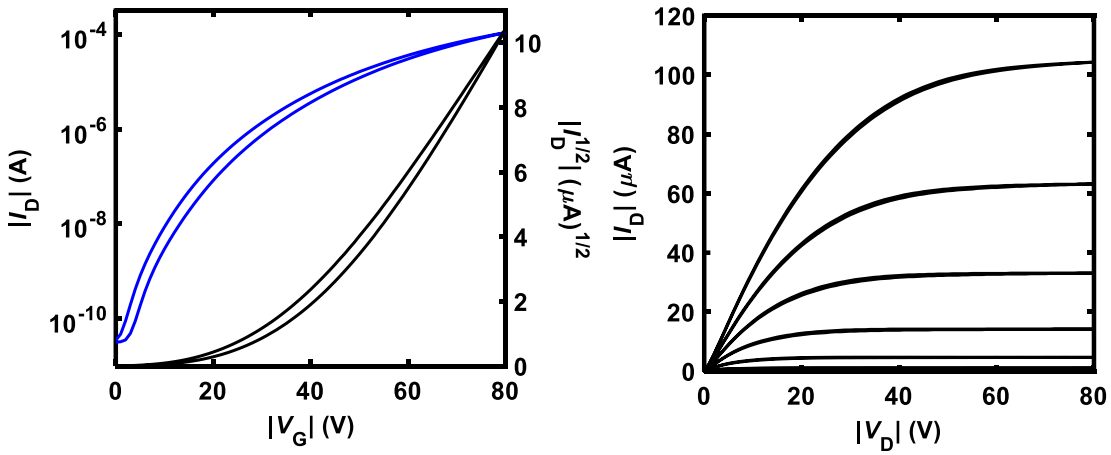


***Figure* 1.6.** *a) transfer and b) output characteristic of an OFET device. The transfer characteristic shows: firstly, the cut-off region existing when* $|V_{GS}| < |V_{TH}|$ *then shows the saturation regime. The output curve shows, firstly, that the source-drain current is linear when* $|V_{DS}| < |V_{GS}|$*. Secondly, the saturation regime beginning when* $|V_{DS}| \geq |V_{GS}|$*. The source-drain current is in this situation constant because it is independent on the source-drain voltage.*

Parameter Extraction in the Linear Regime

It was written previously that the source-drain currents of OFETs can be described with the MOSFET models, despite a different principle of operation. For this reason, the expression of the source-drain current I_{DS} in the linear regime is as follows:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1.9}$$

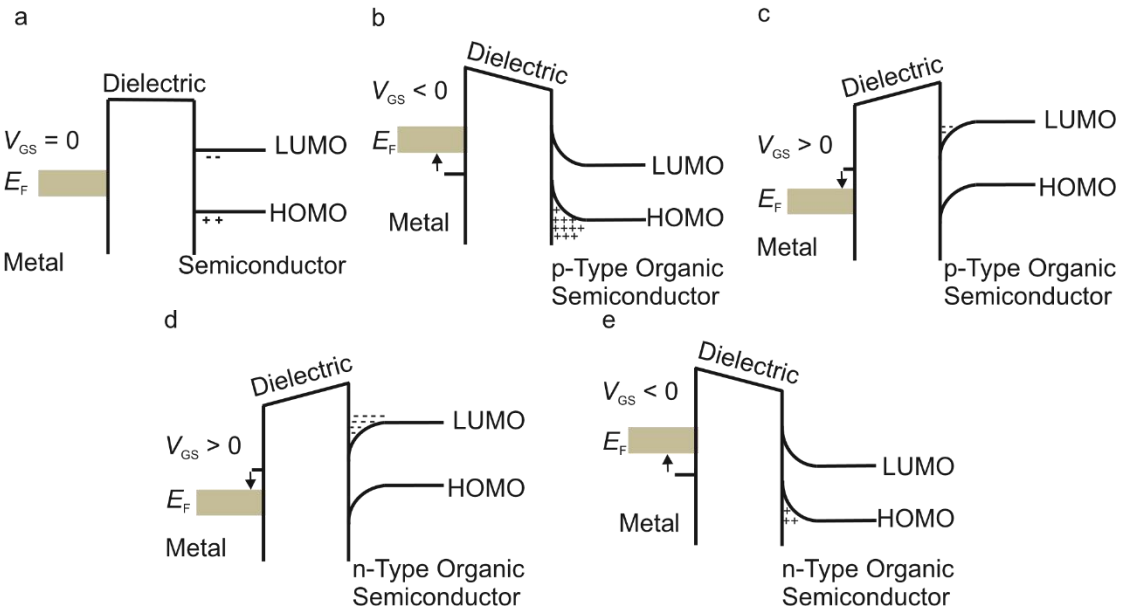


***Figure* 1.7** *Band diagram at the insulator/semiconductor interface dependent on gate bias: a) Band diagram at the interface in the absence of a gate bias. b) For a p-type semiconductor, a negative bias leads to an accumulation of holes at the interface and c) a positive gate bias accelerated the holes towards the semiconductor bulk and the interface is depleted. d) For an n-type semiconductor, the accumulation of the electrons occurs for positive gate voltage and e) the depletion for negative gate bias*.

Where L and W are the length and the width of the channel, C the capacitance of the insulating layer, μ the field effect mobility, V_{DS} and V_{GS} are the drain and the gate voltages and V_T the threshold voltage. The transconductance g_m is given as:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}} = \frac{\mu C_{ox} W}{L} V_{DS} \tag{1.10}$$

The field effect mobility has the form:

$$\mu = \frac{g_m}{C_{ox} W V_{DS}} L \tag{1.11}$$

Parameter Extraction in the Saturation Regime

The expression of I_{DS} in the saturation regime is given as following:

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{1.12}$$

Figure 1.6 displays the $I_{DS}^{1/2}$ - V_{GS} characteristic. This characteristic is employed for the determination of the threshold voltage V_T and the field effect mobility μ.

Moreover, V_T is obtained by extrapolation and μ is obtained from the maximum slope $\partial I_{DS}^{1/2} / \partial V_{GS}$ as followings:

$$\mu = \frac{2L}{C_{ox} W} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \tag{1.13}$$

1.2.3 Principal Parameters of OFETs

For OFETs that use novel materials, three quantities are particularly important: field effect mobility, threshold voltage, On/Off ratio and subthreshold swing. These parameters are presented in the following sections.

Field Effect Mobility

The charge carrier mobility μ quantifies the drift velocity v_D of charge carriers when an electric field E is applied (v_D/E) and is, first of all, a bulk property of a material. In a field-effect transistor, the current is flowing close to the interface to

the dielectric and therefore sensitive to interface effects. Consequently, the expression *field-effect mobility* determines the effective charge carrier mobility for the current in the transistor channel, as derived from the electrical characteristics. Different analyses can be carried out, which, however, yield slightly different values for the charge-carrier mobility. One method is to extract the field-effect mobility from the characteristics in the linear regime following equation (1.9), another method is the extraction from the behavior in the saturation regime from equation (1.12). There exist several mechanisms that limit the field effect mobility in OFETs. One important factor is the structural disorder of the organic thin film. Another one is the presence of interface trap states at the insulator/semiconductor interface. Third, metal/semiconductor interface states at the source or drain electrodes can limit the apparent values of the field-effect mobility.

Threshold Voltage

The threshold voltage V_T is the gate voltage that is necessary for the formation of charge carriers in the conduction channel. For its determination in OFETs, the same formulas are commonly used as in MOSFETs although both structures have different operation mode. The threshold voltage in MOSFETs is the minimal voltage that is necessary for the formation of the inversion layer. OFETs work in accumulation mode, and therefore, finite voltages are required to create charge carriers in the channel. The threshold voltage in these structures is strongly influenced by the presence of traps at the dielectric/semiconductor interface. A change of gate voltage may the lead to filling or release of charges in these states, such that the electric field that reaches the semiconducting channel is modified. Another mechanism that shifts V_T are chemical or structural changes in the materials that may occur at different temperatures. They can significantly influence the charge carrier statistics and, as a consequence, the chemical potential.

On/Off Ratio

An important technological figure of merit of a transistor is the On/Off ratio, given as the ratio of the highest source-drain current I_{On} (within the operation window) divided by the minimal current, I_{Off}, when the gate voltage is swept. In order to enhance the On/Off ratio, obviously both the I_{On} can be enhanced and/or I_{Off} can be reduced. The following paragraphs gives more information about both currents.

I_{On}-Current: The source-drain current I_{On} depends on the geometry of the transistor (width W and length L), the mobility μ of charge carriers and the capacitance of the oxide (equation 1.12). Improved I_{On} is achievable by (1) reducing the channel length, (2) increasing the channel width, which leads to a larger injection surface (3) by using an insulator material with an higher dielectric constant (ϱ) and (4) by interface modification of the injecting metal at the source and drain electrodes.

I_{Off}-Current: This current corresponds to the situation when a minimal amount of charge carriers is present in the transistor channel. For low off currents, wide bandgaps are favourable. Furthermore, the absence of states in the bandgap is important. Its value therefore depends on the purity of the semiconductor, but, additionally, on the insulator film that may induce inhomogeneities and trap states.

Subthreshold swing

The subthreshold swing is a feature of a MOSFET's current–voltage characteristic. In the subthreshold region, the drain current behaviour, though being controlled by the gate terminal, is similar to the exponentially decreasing current of a forward biased diode. Therefore a plot of drain current versus gate voltage with drain, source, and bulk voltages fixed will exhibit approximately logaritmic linear behaviour in this MOSFET operating regime. Its slope is the subthreshold slope.

1.2 Organic devices

1.2.1 π-Conjugated system

In chemistry, a conjugated system is a sequence of connected π-orbitals with delocalized electrons in a molecule, that overlap and form an extended wave function, in which electrons are less confined compared to atomic orbitals. This has two important consequences: The extended wave function lowers overall energy of the molecule and increases stability and the electrons can easily be displaced within the conjugated system, which is favorable for charge transport. Conjugation occurs, in particular, by means of alternating single bonds and multiple (double/triple) bonds, most prominently in carbon compounds.

The electronic configuration of a carbon atom is $1s^2 2s^2 2p^2$. The principal quantum number $n = 2$ has 4 electrons distributed in $2s2p$. In the case of a π-conjugated system, electron states are rearranged to $1s^2 2s 2p^3$ and form 4 orbitals composed of three sp^2-orbitals and one p_z-orbital. sp^2-orbitals are coplanar with a deflection angle of 120° and the p_z-orbital is perpendicular to the sp^2-orbitals plane. Furthermore, during the formation of a molecule, the carbon-carbon bonds results in binding the sp^2-orbitals of each carbon atom; the bond of two sp^2-orbitals is called σ-binding. In addition, the p_z-orbitals overlap with their neighbours and form the π-bindings, which are delocalized along the molecule formed. The σ-bonds play an important role for the stability and the formation of the molecule due to its high binding energy [75] [76]. However, the π-bindings due to its extended nature provide an extended and polarizable system [75] [76], which is the conjugated system. The largest conjugated system known is a macroscopic graphene or graphite crystal, but also the smaller sp^2 carbon allotropes, i.e. carbon nanotubes and fullerenes are fully conjugated. Further, conjugated polymers provide large π-conjugated systems.

1.3 Charge Transport in Organic Materials

Depending on the degree of order in organic conductors and semiconductors, two very different regimes of charge transport can be distinguished as extreme cases: quasi-localized band transport and hopping transport. Most experiments with organic conductors, show, however, contributions from both scenarios, and a crossover that may occur when changing temperature.

Quasi-Delocalized Band Transport: In order to understand the intrinsic mechanisms of charge transport in organic materials, it is instructive to investigate ultra-pure organic materials with high crystalline order. In this limit, several experiments have observed that, towards lower temperature, the mobility increases [77]. This qualitatively reproduces the results of common metals, in which inelastic scattering processes freeze out when the temperature is lowered. This is called the limit of band transport. The temperature dependence arises from lattice vibrations (phonons) in these structures that modify the polarization energy of the lattice and leads to the formation of localized charges (polarons). Similar observations were made in monocrystalline thin films of pentacene [78] [79] [80]. In a refined interpretation of these observations, the idea of a delocalized band transport in these systems was changed to a so-called quasi-delocalized band transport, explicitly taking into account the formation of polarons.

Hopping Transport: Conducting polymers unavoidably provide high intrinsic disorder. This has, among other effects, the consequence that the π-π conjugated electron system is intersected in small areas. In addition to the segmentation of the pathway along which charges travel, which introduces tunneling barriers even within the polymer strand, these segments may also differ in energy due to stochastic influence of their local environment. As a consequence, a model in which charge carriers move between localized states

via thermal excitation are appropriate, that is, in particular, the model of hopping transport. Electric measurements have indeed revealed that the charge mobility in these systems increases with increasing the temperature and decreases with decreasing the temperature [81], which corresponds to the hopping transport.

Multiple Trapping and Release (MTR) Transport: The multiple trapping and release (MTR) model was developed for the description of the charge carriers transport in a transistor device that uses a semiconductor with high disordered structure or ordered structure as conductive pathway. MTR combines both hopping transport and delocalized band transport models. In this case, localized states inside the bandgap of the semiconductor interact with the charge carriers injected by the source-drain electrode by trapping and thermal release [78] [82].

1.4 Contact resistance in OFETs

For semiconductors, and equally for organic semiconductors, the choice of the contacting material is of utmost importance. A suitable metal/semiconductor materials combination should provide efficient charge carrier injection without voltage drop. In this case, the resistance of the metal/semiconductor interface should be negligible compared to the total resistance of the device [83]. Electrically, this ideal behavior is characterized by a linear current-voltage characteristic, which is indicative of an *Ohmic contact*. In organic semiconductors, the charge carriers are easily injected by the metal into the semiconductor film, when the LUMO level of a n-type organic semiconductor (Figure 1.8a) or the HOMO level of a p-type organic semiconductor (Figure 1.8b) coincides with the Fermi level (E_F) of a metal [84] [85]. The metal is subsequently considered as a reservoir of charge carriers. In

conventional semiconductors, ohmic behavior can also be enforced by high doping of the semiconductor material. In this present work, carbon-based semiconductors that we have used, were not intentional doped.

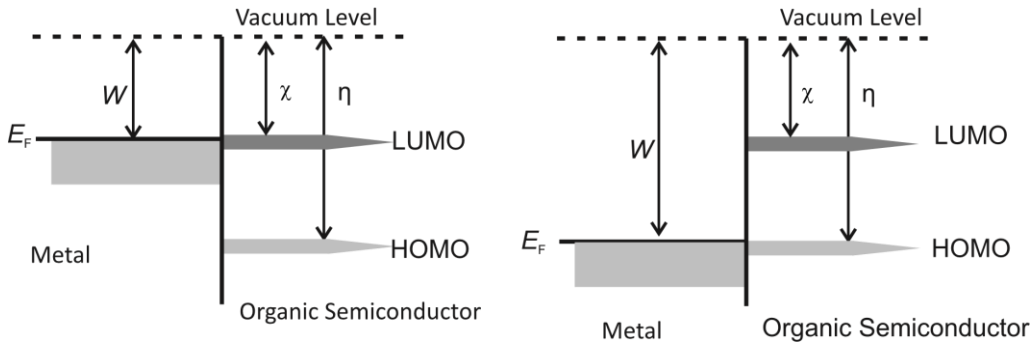


***Figure* 1.8** *Schematic band diagrams of metal and semiconductor. An ohmic behavior can be observed in the device when a) the work function W of the metal and the LUMO of a n-type semiconductor have approximately the same value or when b) W and HOMO of a p-type semiconductor have approximately the same value (χ to the electron affinity and η to the ionization energy of the semiconductor)*.

When the Fermi level of metal and semiconductor are not well aligned, an effective barrier is introduced at the interface. This is illustrated in Figure 1.9, in which the barrier is the result of a non-alignment of the Fermi energy level of the metal with the HOMO level for p-type semiconductor or the LUMO for n-type semiconductor. Two origins of the barrier can be distinguished: first a high energy mismatch between the Fermi level of the metal and the HOMO level for p-type semiconductors or the LUMO level for n-type semiconductor , second the presence of interface states at the metal/semiconductor interface. In both cases, the metal/semiconductor contact is a Schottky-type, which goes along with the formation of a space charge region and a nonlinear injection of charge into the semiconductor, associated with a voltage drop. In simple terms, the contact resistance is then high, and nonlinear.

The general method used for the determination of the contact resistance, R_C, in a OFET device is the transfer line method (TLM). This method consists of measuring the total resistance, R_{on}, for OFETs with various channel lengths. The expression of R_{on} is obtained from the source-drain current in the linear regime at a constant gate voltage (equation 1.14) and given as following:

$$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{V_{GS}} = R_{Ch} + 2R_C \tag{1.14}$$

this results in,

$$R_{on} = \frac{L}{\mu CW(V_{GS} - V_T)} = R_{Ch} + 2R_C \tag{1.15}$$

From the $R_{on}(L)$ characteristic, R_C is obtained by extrapolation at $L = 0$ and the channel resistance R_{Ch} can then be deduced.

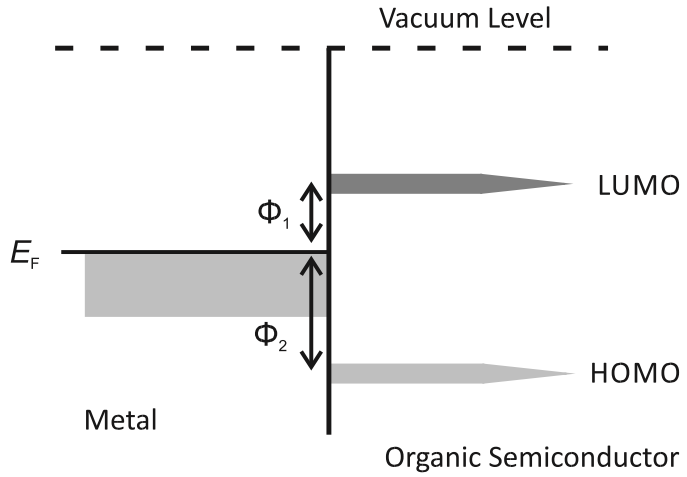


***Figure* 1.9.** *Schottky-type contact in OFET device. It is caused by a nonalignment of metal's Fermi energy with the conduction band (LUMO) or with the valence band (HOMO) of a organic semiconductor. For a n-type organic semiconductor, the barrier height has a value of φ_1. For a p-type semiconductor, the barrier height has a value of φ_2.*

1.5 Mechanisms limiting the transport in OFETs

In this section, we discuss two mechanisms that limit efficient charge transport in OFETs.

1.5.1 Insulator/Semiconductor Interface

The presence of traps at the insulator/semiconductor interface is an important factor that limits the current in OFETs [86] [87]. The term traps indicate that charge carriers, which are contributing to the current, can temporarily be captured in localized states, and subsequently be released. This mechanism reduces the overall charge mobility. Near interface trap states can be characterized by studying the MIS-capacitor, depicted in Figure 1.10a, in which the time dependence of the capture and release process can be studied [88]. Information about the mobile and the fixed charges at the interface and their influence on electrical properties of the semiconductor can be obtained. The structure is fabricated by stacking of metal, insulator and semiconductor materials. It is described an equivalent circuit with two serial capacitances and three resistors as displayed in Figure 1.10b. Each organic layer layer is considered in the circuit as one RC element. The impedance *Z* of such a circuit is given by:

$$Z = Z_R + jZ_C \tag{1.16}$$

Z_R and Z_C are the real part and the imaginary part of the impedance, respectively. The admittance *Y* is defined as:

$$Y = \frac{1}{Z} = G + j\omega C \tag{1.17}$$

The parameters G and C are the conductance and the capacitance, measured as a linear response on a small AC modulation voltage at constant frequency. In addition, the quasi-static DC gate voltage is swept slowly. $G(V)$ and $C(V)$ give access to near interface trap states.

For an ideal MIS-capacitor, the capacitance or the admittance curves form two plateaus. In the $C - V$ characteristic, the lower plateau corresponds to the capacitance in the depletion and is the series sum of the capacitance of insulator film C_{IS} and the capacitance of the semiconductor layer C_{SC}. The higher plateau corresponds to the capacitance in the accumulation regime and is the capacitance of the insulator film C_{IS}. The transition region is governed by near-interface traps. An ideal transition has a steep slope, whereas a broad slope indicates a high density of near-interface traps. The measurement can be extended by variation of frequency. With increasing frequency, the capacitance in accumulation decreases due to the semiconductor resistance R_{SC} and falls towards the depletion capacitance.

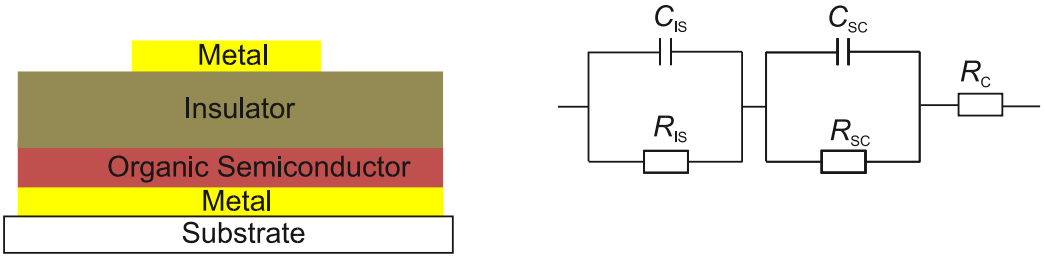


***Figure* 1.10** *MIS-capacitor device. a) The device is obtained by stacking of organic materials. b) Parallel 2RC circuit describing the MIS-capacitor, in which each organic material corresponds to a RC circuit. (R_{SC}, C_{SC}: electrical resistance and capacitance of the semiconductor layer; R_{IS}, C_{IS}: electrical resistance and the capacitance of the insulator layer).*

1.5.2 Schottky-type contact

It was written previously that in the presence of a high barrier, the contact is of Schottky-type. In this situation, the contact resistance R_C can be higher than the bulk resistance R_{SC} and, consequently, be the limiting factor for charge transport. In this case, charge injection in the semiconductor film is described

by two limiting types of emissions. The first is the thermionic emission. In this case, a small fraction of charge carriers overcome the barrier by thermal excitation and are injected into the semiconductor film, when their kinetic energy is sufficient. The second case is field emission. Here, the charge carriers are injected at high electric field by a tunneling mechanism. When the potential barrier in a Schottky contact is relatively large, and at sufficiently high voltage, the thermionic emission is not significant as compared to the field emission. The expression of the tunnel current density j was derived by Fowler and Nordheim [89] and it is given as following:

$$j = AF^2 exp\left(-\frac{\kappa}{F}\right) \tag{1.18}$$

With:

$$A = \frac{e^3}{8\pi h\phi} \quad and \quad \kappa = \frac{8\pi\sqrt{2m}\phi^{3/2}}{3eh} \tag{1.19}$$

Where F is the electric field, e the elementary charge, h the Planck constant, ϕ the barrier height and m the effective mass of the charge carriers.

Chapter 2: Fabrication of organic devices

In this section are described fabrication of FET using organic materials as active layer and the properties of those devices. For instance, a preliminary treatment of the substrate was needed. Then, thermal deposition in a vacuum chamber is the method used for the fabrication of FETs. Finally, the measurements of FET properties were made into a glove box filled with Ar gas.

2.1 Preliminary treatment of substrates

Before the deposition of thin films for FETs and inverters devices, substrates have been subjected of a preliminary treatment in order to avoid leakage current and make them hydrophobic. In case of FET devices, the SiO2/Si and ZrO_2/Si substrate were cleaned through the following steps:

1- The substrate was washed, under ultrasonic irradiation, with acetone and then with methanol for 5 min each to remove organic and inorganic impurities.

2- The SiO_2/Si substrate was washed with ultra-purified water under ultrasonic irradiation for 5 min and the ZrO_2/Si substrate was washed with isopropyl alcohol under ultrasonic irradiation for 5 min.

3- The substrate was immersed into a H_2O_2/H_2SO_4 solution (1:4 in volume ratio) for 1 min to remove organic and inorganic impurities in the SiO_2 and ZrO_2 layer.

4- The substrate was washed with running ultra-purified water for 5 min and left in ultra-purified water for 10 min.

5- The substrate was finally dried by spraying nitrogen (N_2) gas. After the cleaning of the substrate, the surface of the SiO_2/Si substrate was treated with a mixed solution of hexamethyldisilazane (HMDS) and hexane (1:9 in volume ratio) for half a day so that it becomes hydrophobic. The surface of

ZrO_2/Si substrate was covered by 50 nm thick parylene-C (parylene) to avoid leakage current and also to make the surface hydrophobic.

6- The substrate was washed with methanol and then with ultra-purified water under ultrasonic irradiation for 5 min each.
7- The substrate was dried by spraying N_2 gas, and it was heated at 105 °C for 3 min.

In case of plastic substrates, polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), the procedure is different. The plastic substrate was washed with methanol and isopropanol under ultrasonic irradiation for 5 min each, and it was dried by spraying N_2 gas. The plastic substrate was coated with 5 nm thick chromium (Cr) and 100 nm thick gold (Au) to make the gate electrode.

To prepare the SiO_2 substrate of ring oscillators devices for the deposition of materials fewer cleaning steps are required:

1. The SiO2/Si substrate was washed with methanol under ultrasonic irradiation for 5 min to remove impurities.
2. The SiO2/Si substrate was washed with isopropyl alcohol under ultrasonic irradiation for 5 min to remove impurities.
3. The substrate was dried by spraying nitrogen (N_2) gas.

2.2 Devices fabrication

This section explains how to fabricate organic FET using thermal deposition: the depositions of organic materials, dielectric and electrodes are described. Moreover, organic molecules, gate dielectric and substrates used in this study are described. Also, the measurement setup is presented.

2.2.1 Material deposition on substrates

All the deposition process was made into a vacuum chamber (Figure 2.1) where the material sample is connected to a current source, the shutter covers the substrate to prevent undesired deposition.

A common method of thin-film deposition is evaporation (thermal deposition). The source material is evaporated in a vacuum by applying current to the crucible that contains the sample. The vacuum allows vapor particles to travel directly to the target object (substrate), where they condense back to a solid state.

Evaporation involves two basic processes: a hot source material evaporates and condenses on the substrate. It resembles the familiar process by which liquid water appears on the lid of a boiling pot. Evaporation takes place in a vacuum, *i.e.* vapors, other than the source material, are almost entirely removed before the process begins. In high vacuum (with a long mean free path), evaporated particles can travel directly to the deposition target without colliding with the background gas. (By contrast, in the boiling pot example, the water vapor pushes the air out of the pot before it can reach the lid.) Hot objects in the evaporation chamber, such as heating filaments, produce unwanted vapors that limit the quality of the vacuum.

Evaporated materials deposit nonuniformly if the substrate has a rough surface (as integrated circuits often do). Because the evaporated material attacks the substrate mostly from a single direction, protruding features block the evaporated material from some areas. This phenomenon is called "shadowing" or "step coverage."

When evaporation is performed in poor vacuum or close to atmospheric pressure, the resulting deposition is generally non-uniform and tends not to be a continuous or smooth film. Rather, the deposition will appear fuzzy.

To start the deposition a current source was applied; increased gradually until the deposition rate (provided by the thickness meter) reaches 0.1 Å/s. At that point the shutter was opened manually and closed after the thickness had reached the desired value.

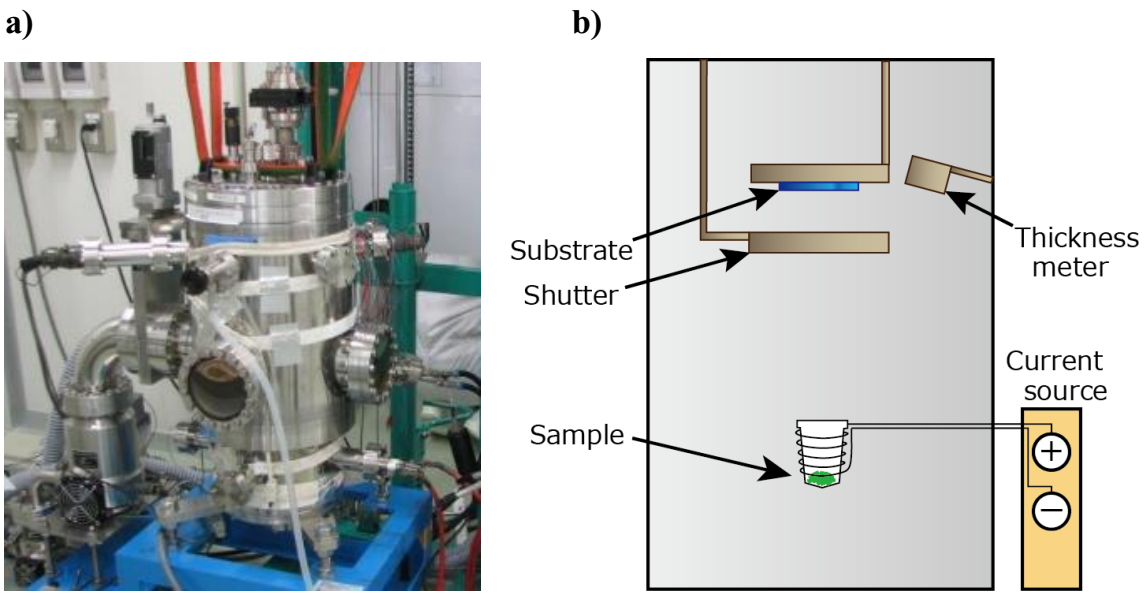


Figure 2.1 *(a) Vacuum chamber for thermal deposition of materials. (b) Internal structure of the vacuum chamber*

The organic materials were deposited on the substrate that was previously treated (Paragraph 2.1). Thin films were formed by the thermal deposition of organic molecules in a chamber (Figure 2.1) where a 10^{-6} Torr vacuum level is maintained. The vacuum level was provided by a rotary pump and other two molecular pumps (PTI-50 and PTI-300). The thickness of the thin films was monitored by using a thickness meter to make 60 nm thick thin films on each gate dielectric.

After thin film deposition, 3 nm thick 2,3,5,6-tetrafluoro-7,7,8,8-teracyano-quinodimethane (F4TCNQ) was deposited on the organic thin films, and the

source and drain electrodes were formed by the thermal deposition of Au on F4TCNQ. The F4TCNQ layer between the Au source/drain electrodes and the organic thin film was introduced to reduce the contact resistance. F4TCNQ is one of the most widely used and most effective p-type dopants due to its strong electron-accepting ability and the extended π system. It has a deep LUMO level (-5.2 eV) which is energetically in the vicinity of the HOMO level of many organic semiconductors.

The dielectrics used in this study are SiO_2 with 400 nm thickness, ZrO_2 with 150 nm thickness and parylene-C (through this thesis, parylene-C is abbreviated 'parylene').

Thickness of SiO_2 was 400 nm. For the flexible FET device, ~1 μm thick parylene was deposited on the Au electrode on plastic substrate. The high-*k* gate dielectric, ZrO_2, with 150 nm thickness was prepared on the plastic substrate by using electron-beam deposition. To avoid the leakage, the surface of ZrO_2 was coated with 50 nm thick parylene.

Parylene, alone, was also used in ring oscillators as gate dielectric with ~600 nm thickness.

2.2.2 Organic material used for devices

As active layer of FET devices [7]phenacene molecules were used. Phenacenes, an isomeric form of acenes and helicenes, have been known as stable compounds in which the benzene rings are fused in a zigzag structure. It was found that phenacene molecules, could serve as an active layer for a high performances *p*-channel organic thin film FET.

In complementary inverters two organic molecules were used for the active layers of the FETs. [7]phenacene were used for *p*-channel FETs, while *N*,*N*'-dioctyl-3,4,9,10-perylenedicarboximide (PTCDIC8) was used for *n*-channel FETs.

In ring oscillators three organic molecules were used: $(C_{14}H_{29})_2$-picene and [6]phenacene were used for *p*-channel FET, while PTCDI-C8 was used for *n*-channel FET. The active layer was formed by the thermal deposition described in section 2.2.1.

2.2.3 Plastic substrates for flexible devices

Two plastic substrates, polyethylene naphthalate (PEN) and polyethylene terephthalate (PET), were used for the flexible FET in this study. PEN and PET are general-purpose thermoplastic polymers which belong to the polyester family of polymers. Polyester resins are known for their excellent combination of properties such as mechanical, thermal, chemical resistance as well as dimensional stability. Both them are highly flexible, colorless and semi-crystalline resin in its natural state. The molecular structures of PEN and PET are shown in Figures 2.2 a) and b), respectively. The plastic substrates are commercially available. In this study, the above plastic substrates with 125 μm thickness were used for the fabrication of flexible complementary inverters.

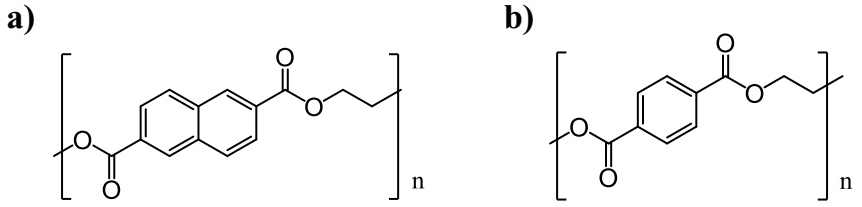


Figure 2.2 *Molecular structures of a) PEN and b) PET.*

2.2.4 Measurement of devices characteristics

All measurements were performed in a two-terminal measurement mode at room temperature using Agilent B1500A semiconductor parametric analyser in an argon (Ar) filled glove box. The measured data were analysed using a Fortran program to determine the fundamental FET parameters such as μ, threshold voltage (V_{TH}), on/off ratio and subthreshold swing (S).

Chapter 3: Organic thin-film FETs

In this chapter the properties of organic devices are shown. Features of OFET, complementary inverters are reported.

3.1 Characterization of organic thin-film FETs

3.1.1 Properties of [7]phenacene thin-film FETS with SiO_2 gate dielectric

In this paragraph properties of [7]phenacene thin-film FETs with SiO_2 gate dielectric are analysed. Device structure showed in Fig. 3.1 and details are showed in Chapter 2; 400 nm thick SiO_2 was used as the gate dielectric. The transfer and output characteristics for the [7]phenacene thin-film FET formed on the SiO2/Si substrate are showed in Fig. 3.1 (a) and (b). Considering that the source voltage, V_S, was 0 V (the source electrode was grounded) the absolute drain current, $|I_D|$, increases upon applying the negative gate voltage, V_G, i.e., $|I_D|$ increases with increasing $|V_G|$. A voltage of -80 V was applied at the drain–source voltage, V_{DS} (= V_D–V_S).

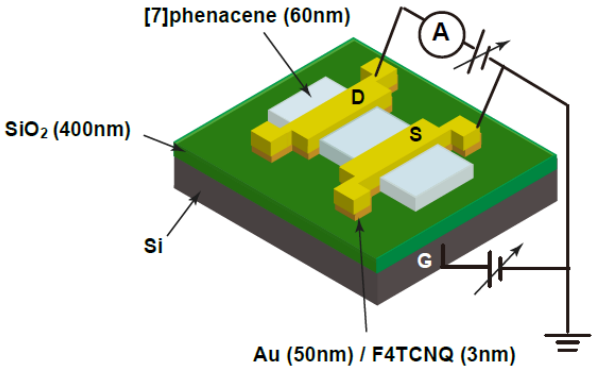


Figure 3.1 *Device structure of [7]phenacene FET whit SiO_2 gate dielectric.*

This transfer curve shows *p*-channel operation, because $|I_D|$ increases by applying negative V_G. The output characteristics, the $|I_D|$–$|V_D|$ plot, at different

negative V_G values exhibited typical normally-off properties. The values of μ, $|V_{th}|$, on/off ratio and subthreshold swing are showed in Table 3.1.

The values of μ, $|V_{th}|$, on/off ratio and SS obtained from five [7]phenacene thin-film FET devices are listed in Table 3.1. The average values of μ, $|V_{th}|$, on/off ratio, and SS obtained from the four devices were 0.91 $cm^2 V^{-1} s^{-1}$, 29.6 V, 6.76 × 10^6 and 3 V $decade^{-1}$, respectively. In addition, the capacitance per area, C_0, for 400 nm thick SiO_2 was 8.34 nF cm^2, which was determined from the extrapolation of C_0 recorded from 20–1000 Hz to 0 Hz.

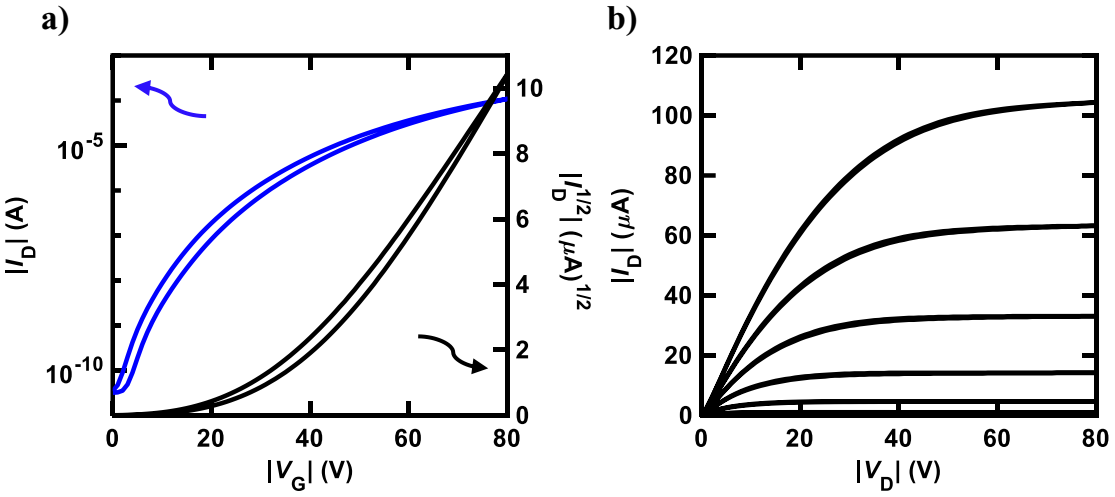


Figure 3.2 *a) transfer and b) output curve of [7]phenacene thin-film FET. V_{DD} = -80 V.*

Table 3.1 *FET parameters of [7]phenacene thin-film FET with SiO_2 gate. V_{DD} = -80 V.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\|V_{th}\|$ (V)	*ON/OFF*	*S* (V/decade)	*L* (μm)	*W* (μm)
#1	8.40×10^{-1}	24.0	1.43×10^5	3.34	450	1000
#2	1.20	33.4	3.11×10^6	3.50	50	500
#3	7.76×10^{-1}	30.2	9.80×10^5	3.40	250	500
#4	1.14	30.8	1.65×10^7	2.12	50	500
#5	6.12×10^{-1}	29.5	1.30×10^7	2.65	250	500
average	$9(3)\times10^{-1}$	30(3)	$7(8)\times10^6$	3.0(6)		

3.1.2 Properties of [7]phenacene thin-film FETs with ZrO_2 gate dielectric

In this section, the FET characteristics of [7]phenacene thin-film FETs with ZrO_2 gate dielectric are fully described. A typical device structure is shown in Fig. 3.3 and details are showed in Chapter 2. Fig. 3.4 (a) and (b) show the transfer and output characteristics of the [7]phenacene thin-film FET formed on the 150 nm thick ZrO_2 gate dielectric. The surface of the ZrO_2 layer was covered with 50 nm thick parylene to produce the hydrophobic surface and avoid the leakage current.

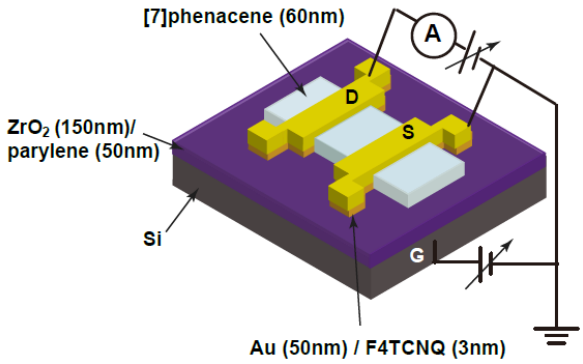


Figure 3.2 *Device structure of [7]phenacene FET whit ZrO_2 gate dielectric.*

$|I_D|$ increases upon applying the negative gate voltage V_G, *i.e.*, $|I_D|$ increases with increasing $|V_G|$, in which the V_D was fixed at -16 V (V_{DS} = -16 V). The transfer curve implies typical *p*-channel operation. The $|I_D|$-$|V_D|$ plots at different negative V_G values exhibited typical normally-off properties. The values of μ, $|V_{th}|$, on/off ratio and SS obtained from five [7]phenacene thin-film FET devices are listed in Table 3.2 The average values of μ, $|V_{th}|$, on/off ratio, and SS obtained from the four devices were 0.21 $cm^2\ V^{-1}\ s^{-1}$, 6.7 V, 2.07×10^5 and 0.27 V $decade^{-1}$, respectively. The μ value is lower than that in the [7]phenacene thin-film FET described in Paragraph 3.1.1. Moreover, the $|V_{th}|$ value is quite small, indicating the high-performance/low-voltage operation. In addition, the capacitance per area, C_0, for the dielectric was 38.9 nF cm^2, which was determined from the

extrapolation of C_0 recorded from 20–1000 Hz to 0 Hz. Thus, the [7]phenacene thin-film FET device formed on the ZrO_2 substrate showed excellent FET properties, demonstrating that [7]phenacene is a promising material as a OFET.

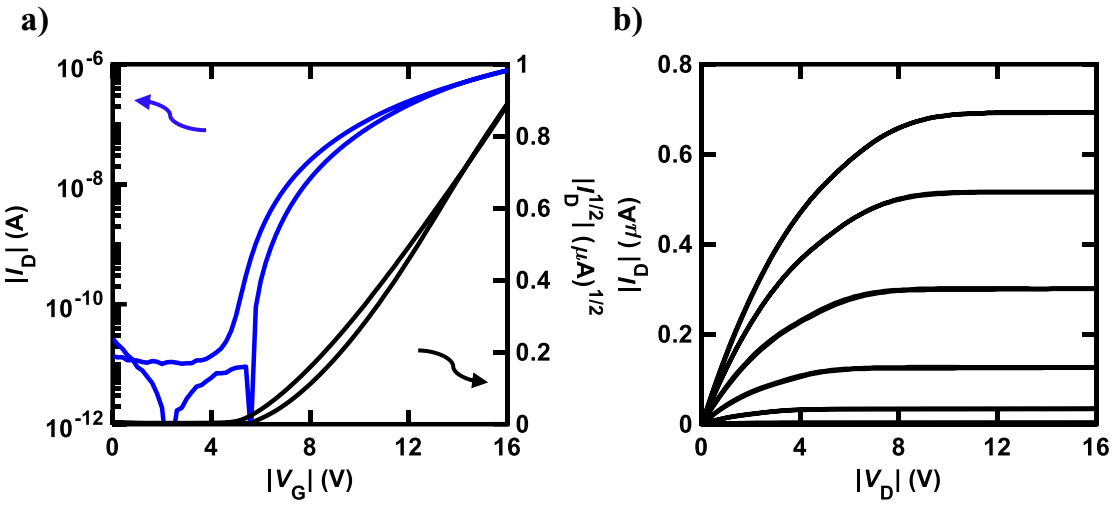


Figure 3.4 *a) transfer and b) output curve of [7]phenacene thin-film FET. V_{DD} = -16 V.*

Table 3.2 *FET parameters of [7]phenacene thin-film FET with ZrO_2 gate. V_{DD} = -16 V.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	2.73×10^{-1}	7.75	7.93×10^{5}	0.29	450	1000
#2	2.62×10^{-1}	6.64	9.79×10^{5}	0.22	450	1000
#3	2.51×10^{-1}	5.26	1.23×10^{6}	0.13	450	1000
#4	1.29×10^{-1}	6.95	3.97×10^{5}	0.33	250	500
#5	1.19×10^{-1}	6.94	2.07×10^{5}	0.27	450	500
average	$2.1(7)\times10^{-1}$	6.7(9)	$7(4)\times10^{5}$	$2.7(8)\times10^{-1}$		

3.2 Characterization of organic CMOS inverters

In previous paragraph, *p*-channel OFETs with high electrical performance, low operation voltage, and good operational stability are obtained.

Inverter (NOT circuit) is one of the fundamental building blocks in digital circuits. It is commonly represented in the form of a pull-down and a pull-up element switching the inverter output to ground (GND) or to the supply voltage (V_{DD}) via a low resistance path.

The equivalent circuit of complementary MOS (CMOS) inverter is shown in Figure 3.5 a). The research work involves the integration of *n*-channel and *p*-channel OFETs with comparable performance into complementary inverters.

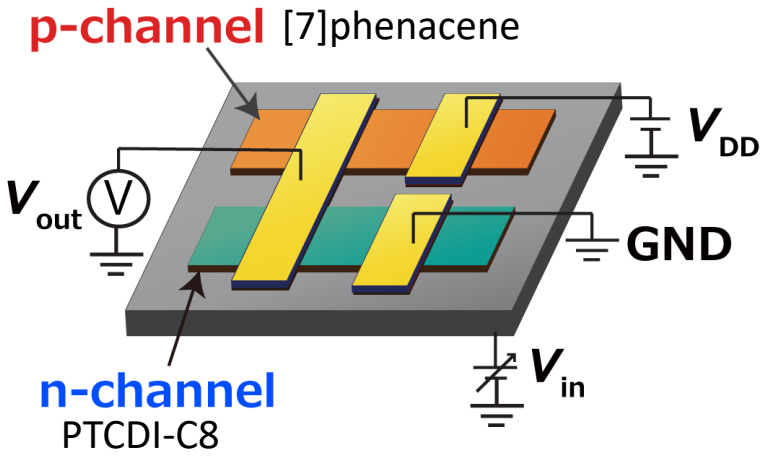


Figure 3.5 *Device structure of [7]phenacene/PTCDI-C8 CMOS inverter.*

The operation of a CMOS inverter can be readily understood from a simplified circuit model. The OFETs function in a manner similar to a switch with a finite on-resistance R_{on}. When V_{in} is high (or equal to V_{DD}), the *n*-channel OFET is on (with a finite on-resistance R_{on}), while the *p*-channel OFET is off (the switch is open). A conductive path is formed between the output node and the ground node, resulting in a low output voltage of 0 V. On the other hand, when the input is low (or equal to 0 V), the *p*-channel OFET is on and the *n*-channel OFET is off. A conductive path between the supply voltage (V_{DD}) and the output voltage (V_{out}) is

formed, leading to a high output voltage. There will never be a conducting path between the supply and ground under steady-state operation. Consequently, there is no static power consumption in CMOS inverters except for small power dissipation due to leakage current.

The ideal V_{out} - V_{in} curve is shown in Figure 3.6 b). The gain is defined as dV_{out}/dV_{in} as shown in Figure 3.6 b).

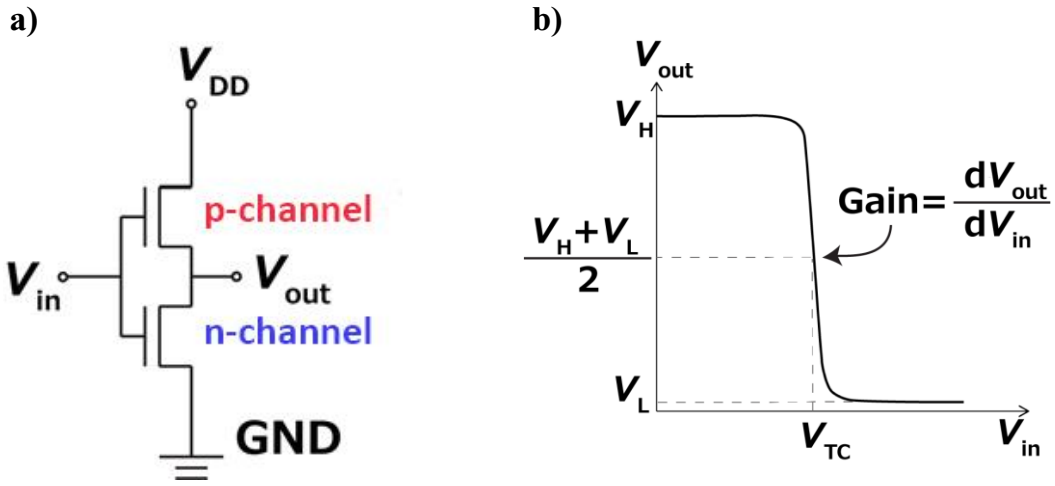


Figure 3.6 *a) Equivalent circuit and b) ideal $V_{out} - V_{in}$ curve of CMOS inverter.*

In this section, the author fabricated the CMOS inverter which is composed of [7]phenacene thin-film FET as *p*-channel FET and PTCDI-C8 thin-film FET as *n*-channel. The CMOS inverter was fabricated on Si, PET and PEN substrates with three different gate dielectric: SiO_2, ZrO_2 and parylene. The inverter was fabricated according to the following process: (1) 60 nm thick [7]phenacene thin films were formed to produce the *p*-channel active layers. (2) 60 nm thick and PTCDI-C8 thin films were formed to produce the *n*-channel active layers. (3) 3 nm thick F4TCNQ and 100 nm thick Au source and drain electrodes were finally formed. In case of plastic substrates, 100 nm thick Au gate electrode was formed on PET/PEN covered with 5 nm thick Cr and 1 μm thick parylene film was formed as gate dielectric on Au/Cr/PET substrate.

Therefore, *p*-channel and *n*-channel FETs are connected by Au electrode, where V_{out} is measured. The V_{in} is applied to the gate electrode.

3.2.1 Features of CMOS inverter

Switching Threshold Voltage

The switching threshold voltage V_{TC} is an important parameter that characterizes the steady-state input-output behavior of CMOS inverter circuits. V_{TC}, defined as the point V_{in} which provides $V_{out} = (V_H - V_L)/2$. The ideal case is when $V_{TC} = V_{DD}/2$. V_{TC} can be identified graphically at the intersection of the inverter curve and the line given by V_{in} = 50 V. Setting the inverter threshold voltage to a desired voltage value is very important in the design of CMOS inverters. For long-channel transistors, the channel-length modulation factor (λ) can be ignored. Then, the switching threshold voltage can be calculated from the performance parameters of the transistors:

$$V_{TC} = \frac{V_{DD} - |V_{THp}| + V_{THn}\sqrt{k_R}}{1 + \sqrt{k_R}} \tag{3.1}$$

where V_{THn} and V_{THp} are the threshold voltage of the n- and *p*-channel OFETs, respectively, and k_R is the ratio of the current gain factors ($k_R = k_n/k_p$) between n- and *p*-channel OFETs. The current gain factors are defined as follows:

$$k_n = \frac{\mu_n C_{ox} W_n}{L_n} \tag{3.2}$$

$$k_p = \frac{\mu_p C_{ox} W_p}{L_p} \tag{3.3}$$

Gain

The signal gain of the inverters equals the gain at the switching threshold V_{TC}. A high gain in the transition region is very desirable. The gain can be easily extracted from the inverter curve by calculating the derivative of V_{out} over V_{in}. The gain primarily depends on the transconductances of the n- and *p*-channel OFETs at the midpoint voltage of the inverter. The static CMOS inverter can also be used as an analog amplifier, as it has a high gain in its transition region. This region, however, is very narrow as shown in Figure 3.7 b). The highest gain corresponds to the switching threshold voltage V_{TC}.

3.2.2 Properties of [7]phenacene/PTCDI-C8 organic complementary inverter with SiO_2 gate dielectric

In this section are described the properties of complementary inverters made by using [7]phenacene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs. The inverters were fabricated in a top-contact configuration, as shown in Figure 3.7 with connections between transistors leading to the corresponding circuit schematic shown in Figure 3.6 a). 400 nm thick SiO_2 gate dielectric was used. Table 3.3 show 4 complementary inverter properties.

Table 3.3 *Parameters of [7]phenacene/PTCDI-C8 CMOS inverters.* V_{DD} *= 100 V.*

device	V_{TC} (V)	*Gain*	*L* (µm)	*W* (µm)
#1	42.6	14.8	100	500
#2	71.7	148.5	200	500
#3	87.8	36.1	200	500
#4	87.3	27.2	300	500

As shown in the circuit diagram in Figure 3.6 a), the drain terminals of the two

OFETs were connected to form the output node (V_{out}) of the inverter. A supply voltage (V_{DD}) was applied to the source of the *p*-channel OFETs while the source of *n*-channel was grounded (V_S=0).

The voltage transfer characteristics (VTC) with a supply voltage of V_{DD}=100 V is shown in Figure 3.8 a). The switching voltage V_{TC} was obtained graphically from the intersection of the VTC with the line V_{out} = 50 V (half of V_{DD}=100 V). The maximum dc voltage gain, defined as dV_{out}/dV_{in}, reached is 148.5 and the relative V_{TC} is 71.7 V. Thus, the high-performance CMOS inverter circuit was successfully fabricated using thin films of [7]phenacene and PTCDI-C8.

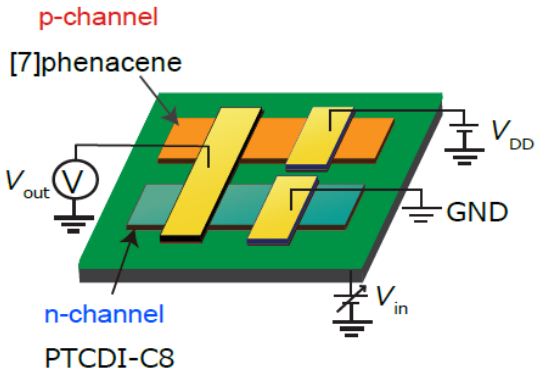


Figure 3.7 *Device structure of [7]phenacene/PTCDI-C8 CMOS inverter with SiO_2 gate dielectric.*

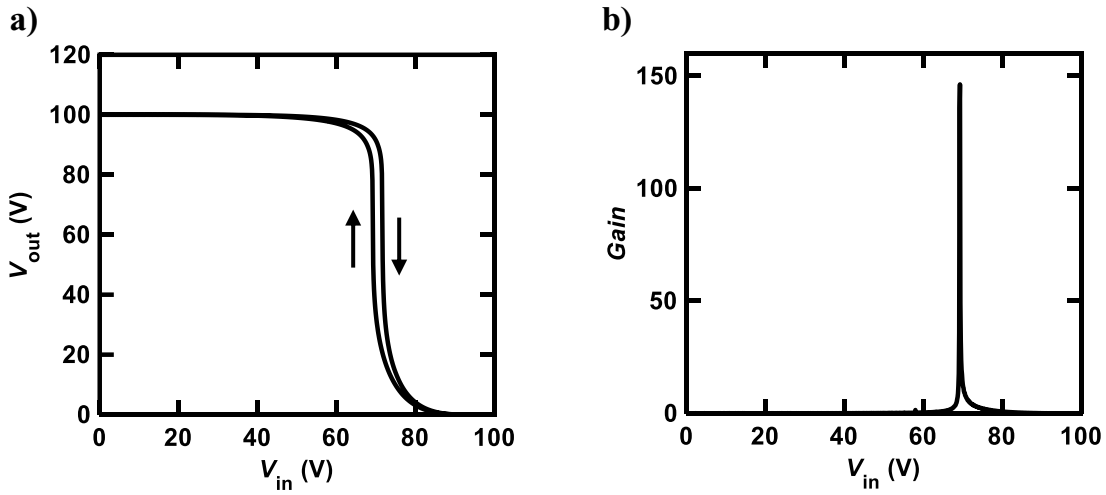


Figure 3.8 *a) V_{out} – V_{in} plots and b) gain at V_{DD}=100 V for [7]phenacene/PTCDI-C8 CMOS inverter formed on Si. SiO_2 was used as gate dielectric.*

Figures 3.9 a) and b) show the transfer and the output curves for [7]phenacene and thin-film FETs which constitutes the *p*-channel FET in CMOS inverter. Figures 3.9 c) and d) show the transfer and the output curves for PTCDI-C8 and thin-film FETs which constitutes the *n*-channel FET in CMOS inverter. The *L* and *W* for both FETs were 200 and 500 µm, respectively. In Tables 3.4 a) and b) FET properties of all four inverters presented in Table 3.3 and are reported.

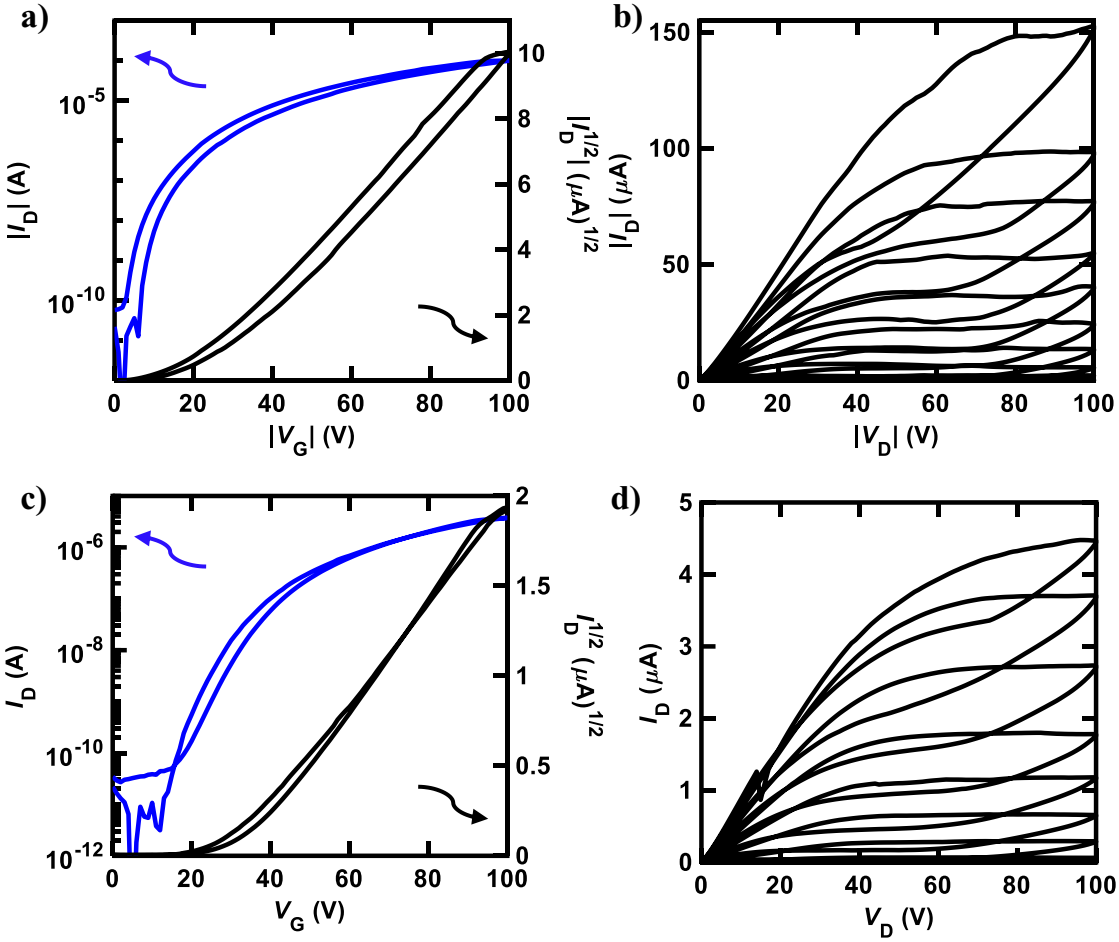


Figure 3.9 *a) Transfer and b) output curves of [7]phenacene thin-film FET used as p-channel FET in CMOS inverter; c) transfer and d) output curves of PTCDI-C8 thin fil FET used as n-channel FET in CMOS inverter. Complementary inverter was formed on Si substrate. SiO_2 was used as gate dielectric. V_{DD}=100.*

Table 3.4 a) *FET parameters of [7]phenacene thin-film FET used in CMOS inverter with SiO_2 gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	2.01	63.3	5.77×10^7	1.59	100	500
#2	1.87	28.4	9.99×10^7	1.04	200	500
#3	0.83×10^{-1}	47.1	2.58×10^7	1.69	200	500
#4	1.76	27.8	6.40×10^7	1.23	300	500

Table 3.4 b) *FET parameters of PTCDI-C8 thin-film FET used in CMOS inverter with SiO_2 gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	8.36×10^{-2}	52.1	4.01×10^6	3.38	100	500
#2	7.80×10^{-2}	30.9	3.75×10^6	3.69	200	500
#3	6.48×10^{-2}	32.4	461	14.28	200	500
#4	8.07×10^{-2}	22.2	2.98×10^5	2.18	300	500

3.2.3 Properties of [7]phenacene/PTCDI-C8 organic complementary inverter with ZrO_2 gate dielectric

In this section are described the properties of complementary inverters made by using [7]phenacene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs. The inverters were fabricated in a top-contact configuration, as shown in Figure 3.10 with connections between transistors leading to the corresponding circuit schematic shown in Figure 3.6 a). 150 nm thick ZrO_2 gate dialectric was used plus 50 nm thick parylene. Table 3.5 show 4 complementary inverter properties.

As shown in the circuit diagram in Figure 3.6 a), the drain terminals of the two OFETs were connected to form the output node (V_{out}) of the inverter. A supply voltage (V_{DD}) was applied to the source of the *p*-channel OFETs while the source of *n*-channel was grounded (V_S=0).

Table 3.5 *Parameters of [7]phenacene/PTCDI-C8 CMOS inverter with ZrO_2 gate dielectric. V_{DD}=18 V.*

device	V_{TC} (V)	*Gain*	*L* (µm)	*W* (µm)
#1	7.6	130.5	100	500
#2	7.3	107.0	100	500
#3	7.7	90.1	200	500
#4	7.9	67.6	300	500

The voltage transfer characteristics (VTC) with a supply voltage of V_{DD}=100 V is shown in Figure 3.11 a). The switching voltage V_{TC} was obtained graphically from the intersection of the VTC with the line V_{out} = 8 V (half of V_{DD} = 16 V). The maximum dc voltage gain, defined as dV_{out}/dV_{in}, reached is 130.5 and the relative V_{TC} is 7.6 V. Thus, the high-performance CMOS inverter circuit was successfully fabricated using thin films of [7]phenacene and PTCDI-C8.

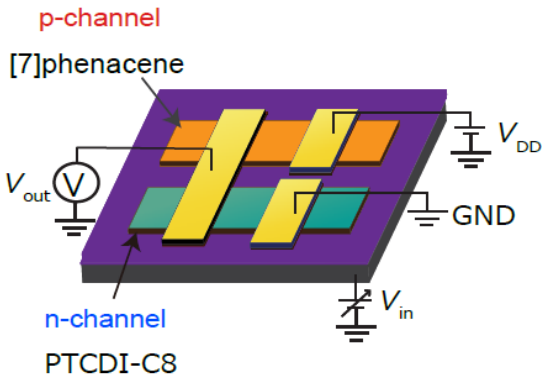


Figure 3.10 *Device structure of [7]phenacene/PTCDI-C8 CMOS inverter with ZrO_2 gate dielectric.*

Figures 3.12 a) and b) show the transfer and the output curves for [7]phenacene and thin-film FETs which constitutes the *p*-channel FET in CMOS inverter. Figures 3.12 c) and d) show the transfer and the output curves for PTCDI-C8 and thin-film FETs which constitutes the *n*-channel FET in CMOS inverter. The *L* and *W* for both FETs were 100 and 500 µm, respectively. In Tables 3.6 a) and b) FET properties of all four inverters presented in Tables 3.5 and are reported.

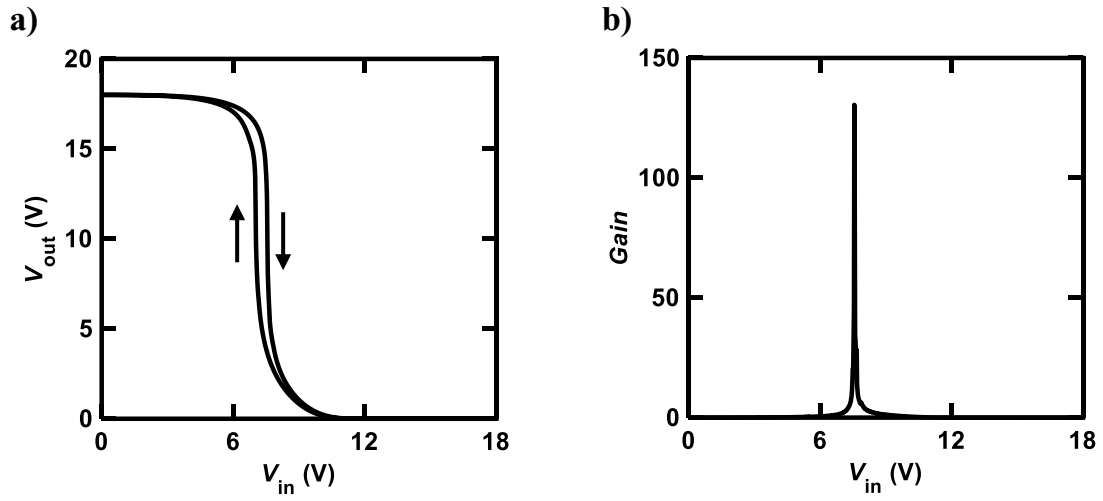


Figure 3.11 *a) $V_{out} - V_{in}$ plots and b) gain at V_{DD}=18 V for [7]phenacene/PTCDIC8 CMOS inverter formed on Si substrate. ZrO_2 was used as gate dielectric.*

Table 3.6 a) *FET parameters of [7]phenacene thin-film FET used in CMOS inverter with ZrO_2 gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	6.72×10^{-1}	7.9	6.48×10^{6}	0.32	100	500
#2	5.03×10^{-1}	10.2	2.98×10^{6}	0.33	100	500
#3	6.62×10^{-1}	7.4	3.55×10^{6}	0.31	200	500
#4	6.91×10^{-1}	7.4	2.48×10^{6}	0.23	300	500

Table 3.6 b) *FET parameters of PTCDI-C8 thin-film FET used in CMOS inverter with ZrO_2 gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th} \rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	8.34×10^{-2}	2.7	1.91×10^{4}	0.94	100	500
#2	8.34×10^{-2}	3.4	2.18×10^{4}	0.78	100	500
#3	8.54×10^{-2}	2.4	9.86×10^{3}	1.04	200	500
#4	8.72×10^{-2}	2.9	1.03×10^{4}	0.97	300	500

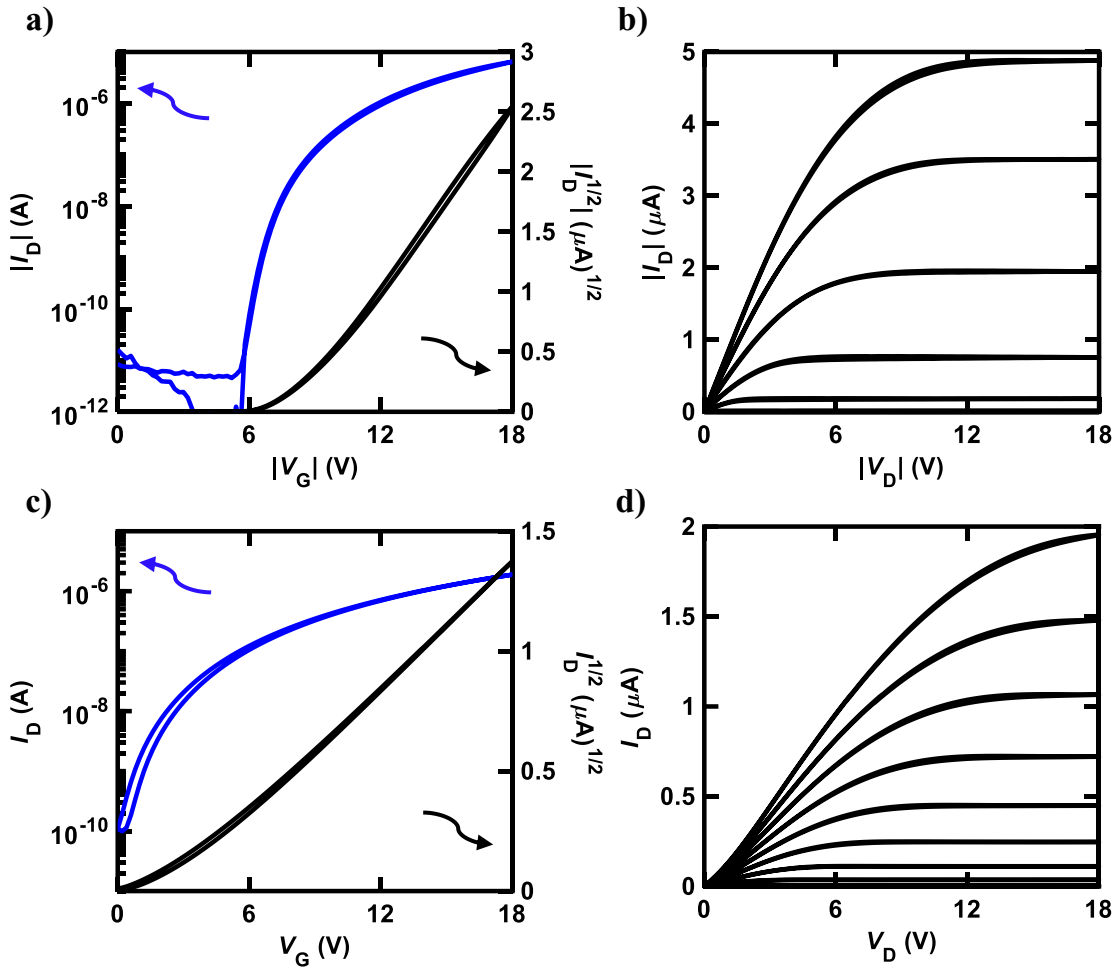


Figure 3.12 *a) Transfer and b) output curves of [7]phenacene thin-film FET used as p-channel FET in CMOS inverter; c) transfer and d) output curves of PTCDI-C8 thin fil FET used as n-channel FET in CMOS inverter. Complementary inverter formed on Si substrate. ZrO_2 was used as gate dielectric. V_{DD}=100.*

3.2.4 Properties of [7]phenacene/PTCDI-C8 organic complementary inverter on PET substrate

In this section are described the properties of complementary inverters made by using [7]phenacene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs, formed on 125 μm thick PET substrate. The inverters were fabricated in a top-contact configuration, as shown in Figure 3.13 with connections between transistors leading to the corresponding circuit schematic

shown in Figure 3.6 a). 1 μm thick parylene was used as gate dialectric. Table 3.7 show 4 complementary inverter properties.

Table 3.7 *Parameters of [7]phenacene/PTCDI-C8 CMOS inverter formed on PET substrate with parylene gate dielectric. V_{DD}=100 V.*

device	V_{TC} (V)	*Gain*	*L* (μm)	*W* (μm)
#1	33.4	155.1	100	500
#2	37.2	146.3	100	500
#3	34.8	136.5	200	500
#4	36.1	135.9	200	500

As shown in the circuit diagram in Figure 3.6 a), the drain terminals of the two OFETs were connected to form the output node (V_{out}) of the inverter. A supply voltage (V_{DD}) was applied to the source of the *p*-channel OFETs while the source of *n*-channel was grounded (V_{S}=0).

The voltage transfer characteristics (VTC) with a supply voltage of V_{DD}=100 V is shown in Figure 3.13 a). The switching voltage V_{TC} was obtained graphically from the intersection of the VTC with the line V_{out} = 50 V (half of V_{DD}=100 V). The maximum dc voltage gain, defined as $dV_{\text{out}}/dV_{\text{in}}$, reached is 155.1 and the relative V_{TC} is 33.4 V. Thus, the high-performance CMOS inverter circuit was successfully fabricated using thin films of [7]phenacene and PTCDI-C8.

Figures 3.14 a) and b) show the transfer and the output curves for [7]phenacene and thin-film FETs which constitutes the *p*-channel FET in CMOS inverter. Figures 3.14 c) and d) show the transfer and the output curves for PTCDI-C8 and thin-film FETs which constitutes the *n*-channel FET in CMOS inverter. The *L* and *W* for both FETs were 100 and 500 μm, respectively. In Tables 3.8 a) and b) FET properties of all four inverters presented in Tables 3.7 and are reported.

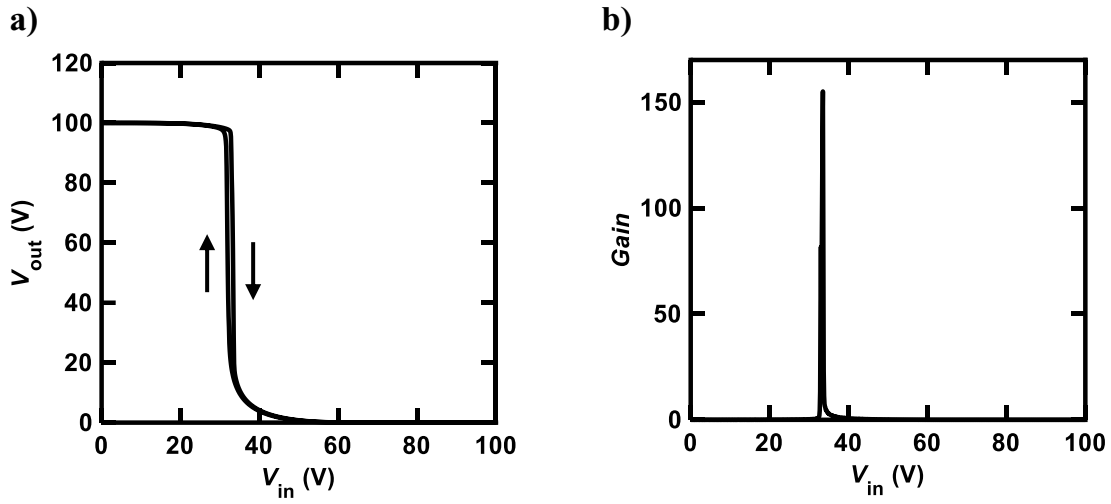


Figure 3.13 *a) V_{out} – V_{in} plots and b) gain at V_{DD}=100 V for [7]phenacene/PTCDIC8 CMOS inverter formed on PET substrate. Parylene was used as gate dielectric.*

Table 3.8 a) *FET parameters of [7]phenacene thin-film FET used in CMOS inverter formed on PET substrate with parylene gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	6.19×10^{-2}	50.7	9.89×10^{5}	2.41	100	500
#2	1.86×10^{-1}	57.7	2.19×10^{6}	3.15	100	500
#3	2.75×10^{-1}	57.1	1.67×10^{6}	2.43	200	500
#4	3.35×10^{-1}	57.1	2.03×10^{6}	3.09	200	500

Table 3.8 b) *FET parameters of PTCDI-C8 thin-film FET used in CMOS inverter inverter formed on PET substrate with parylene gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	9.54×10^{-2}	29.1	1.05×10^{5}	4.99	100	500
#2	1.09×10^{-1}	38.8	7.83×10^{4}	9.01	100	500
#3	9.05×10^{-2}	28.2	4.34×10^{4}	5.88	200	500
#4	8.99×10^{-2}	30.2	3.72×10^{4}	7.70	200	500

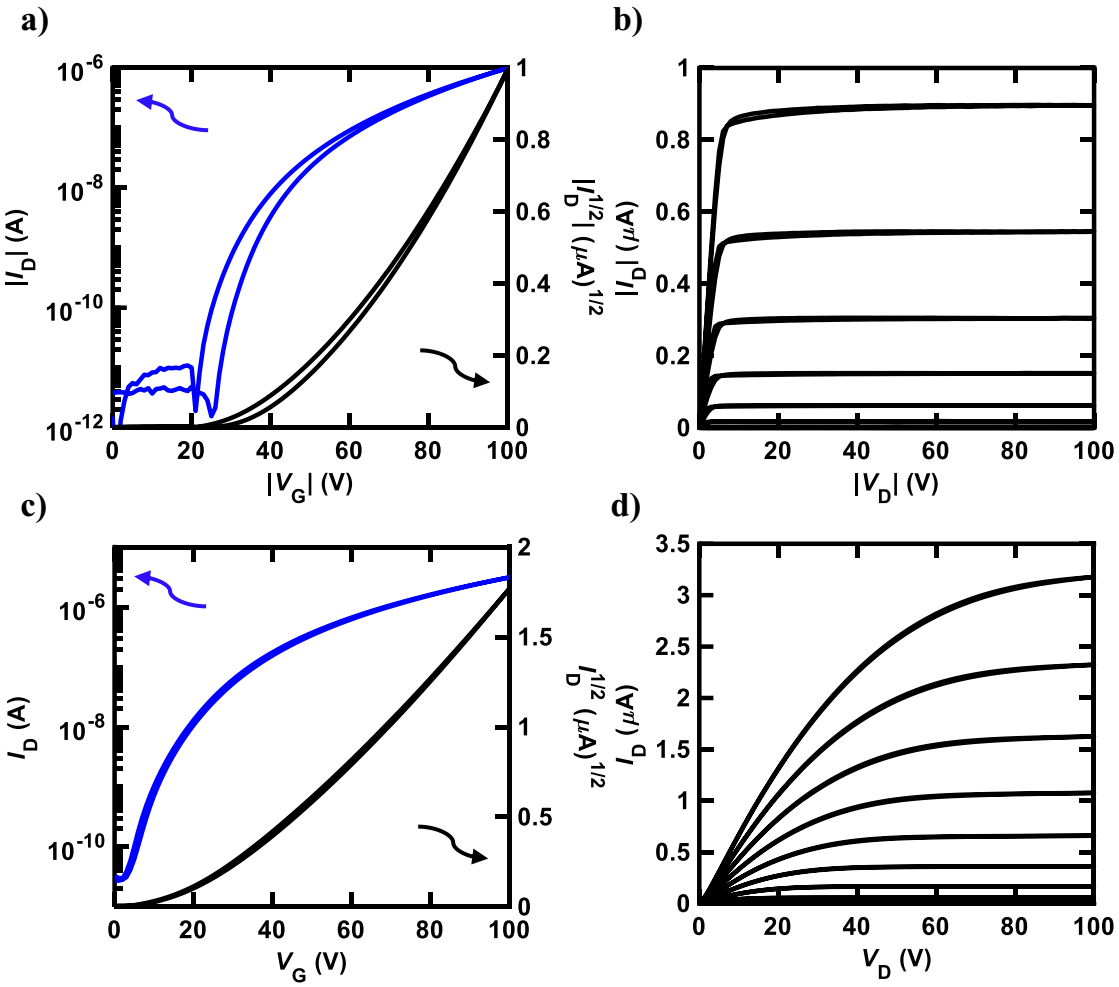


Figure 3.14 *a) Transfer and b) output curves of [7]phenacene thin-film FET used as p-channel FET in CMOS inverter; c) transfer and d) output curves of PTCDI-C8 thin fil FET used as n-channel FET in CMOS inverter. Complementary inverter formed on PET substrate. Parylene was used as gate dielectric.* V_{DD}*=100.*

3.2.5 Properties of [7]phenacene/PTCDI-C8 organic complementary inverter on PEN substrate

In this section are described the properties of complementary inverters made by using [7]phenacene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs, formed on 125 μm thick PEN substrate The inverters were fabricated in a top-contact configuration, as shown in Figure 3.13 with connections between transistors leading to the corresponding circuit schematic

shown in Figure 3.6 a). 1 μm thick parylene was used as gate dialectric. Table 3.9 show 4 complementary inverter properties.

Table 3.9 *Parameters of [7]phenacene/PTCDI-C8 CMOS inverter formed on PEN substrate with parylene gate dielectric. V_{DD}=100 V.*

device	V_{TC} (V)	*Gain*	*L* (μm)	*W* (μm)
#1	31.8	304.7	100	500
#2	34.7	137.5	200	500
#3	37.3	152.8	200	500
#4	37.5	125.7	300	500

As shown in the circuit diagram in Figure 3.6 a), the drain terminals of the two OFETs were connected to form the output node (V_{out}) of the inverter. A supply voltage (V_{DD}) was applied to the source of the *p*-channel OFETs while the source of *n*-channel was grounded (V_S=0).

The voltage transfer characteristics (VTC) with a supply voltage of V_{DD}=100 V is shown in Figure 3.16 a). The switching voltage V_{TC} was obtained graphically from the intersection of the VTC with the line V_{out} = 50 V (half of V_{DD}=100 V). The maximum dc voltage gain, defined as dV_{out}/dV_{in}, reached is 304.7 (highest value of all inverter in this study) and the relative V_{TC} is 31.8 V. Thus, the high-performance CMOS inverter circuit was successfully fabricated using thin films of [7]phenacene and PTCDI-C8.

Figures 3.17 a) and b) show the transfer and the output curves for [7]phenacene and thin-film FETs which constitutes the *p*-channel FET in CMOS inverter. Figures 3.17 c) and d) show the transfer and the output curves for PTCDI-C8 and thin-film FETs which constitutes the *n*-channel FET in CMOS inverter. The *L* and *W* for both FETs were 100 and 500 μm, respectively. In Tables 3.10 a) and b) FET properties of all four inverters presented in Tables 3.9 a) and b) are reported.

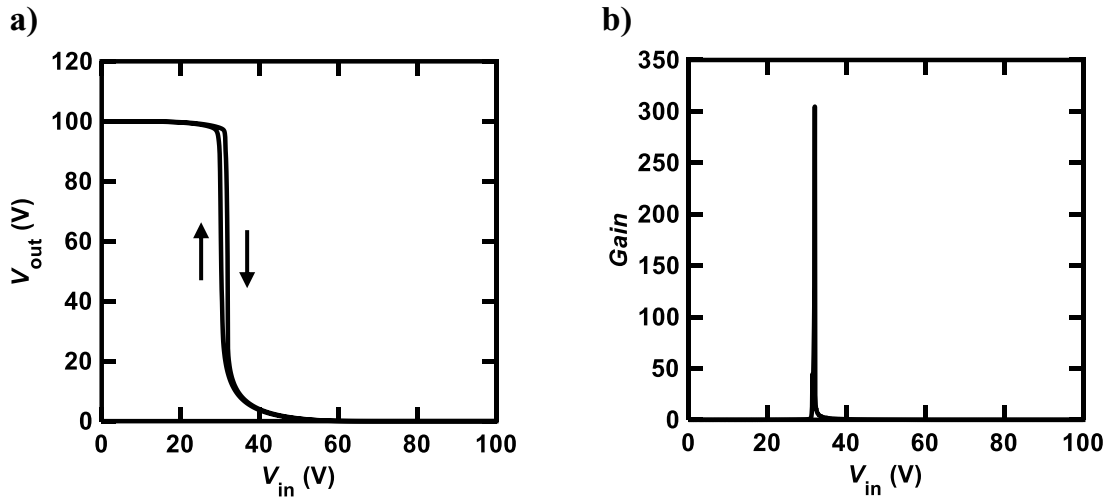


Figure 3.16 *a) V_{out} – V_{in} plots and b) gain at V_{DD}=100 V for [7]phenacene/PTCDIC8 CMOS inverter formed on PEN substrate. Parylene was used as gate dielectric.*

Table 3.10 a) *FET parameters of [7]phenacene thin-film FET used in CMOS inverter formed on PEN substrate with parylene gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	6.19×10^{-2}	50.7	9.89×10^{5}	2.41	100	500
#2	1.86×10^{-1}	57.7	2.19×10^{6}	3.15	200	500
#3	2.75×10^{-1}	57.1	1.67×10^{6}	2.43	200	500
#4	3.35×10^{-1}	57.1	2.03×10^{6}	3.09	300	500

Table 3.10 b) *FET parameters of PTCDI-C8 thin-film FET used in CMOS inverter inverter formed on PEN substrate with parylene gate dielectric.*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)	*L* (µm)	*W* (µm)
#1	9.54×10^{-2}	29.1	1.05×10^{5}	4.99	100	500
#2	1.09×10^{-1}	38.8	7.83×10^{4}	9.01	200	500
#3	9.05×10^{-2}	28.2	4.34×10^{4}	5.88	200	500
#4	8.99×10^{-2}	30.2	3.72×10^{4}	7.70	300	500

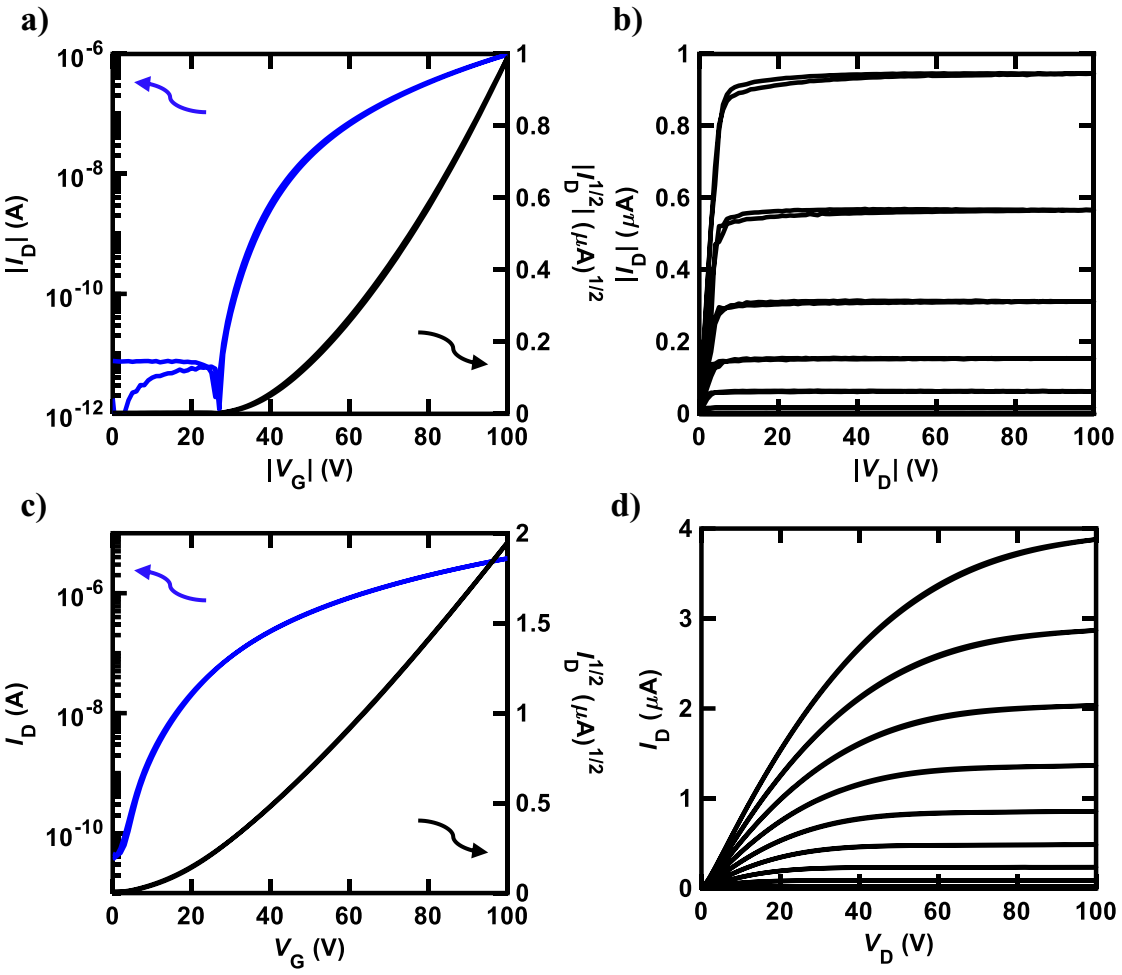


Figure 3.17 *a) Transfer and b) output curves of [7]phenacene thin-film FET used as p-channel FET in CMOS inverter; c) transfer and d) output curves of PTCDI-C8 thin fil FET used as n-channel FET in CMOS inverter. Complementary inverter formed on PEN substrate. Parylene was used as gate dielectric.* V_{DD}*=100.*

Chapter 4: Characterization of ring oscillators

In previous paragraph, organic complementary inverter with high electrical performance, low operation voltage, and good operational stability are obtained. In this chapter we will discuss the characterization of organic ring oscillator. A ring oscillator is a device composed of an odd number of NOT gates in a ring, whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.

Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. The final output is asserted a finite amount of time after the first input is asserted and the feedback of the last output to the input causes oscillation.

A circular chain composed of an even number of inverters cannot be used as a ring oscillator. The last output in this case is the same as the input. However, this configuration of inverter feedback can be used as a storage element and it is the basic building block of static random access memory or SRAM.

A real ring oscillator only requires power to operate. Above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, two methods are commonly used. Firstly, making the ring from a smaller number of inverters results in a higher frequency of oscillation, with about the same power consumption. Secondly, the applied voltage may be increased. In circuits where this method can be applied, it reduces the propagation delay through the chain of stages, increasing both the frequency of the oscillation and the current consumed. The maximum permissible voltage applied to the circuits limits the speed of a given oscillator.

The oscillation frequency f_{osc} results in this study can be explained by the theoretical model described below [74] [90]:

$$f = \frac{1}{2n < \tau_p >} \tag{4.1}$$

where n refers to the number of inverters; is the average τ_p of the ring oscillator; τ_p is expressed by:

$$\tau_p = \frac{(\tau_{pHL} + \tau_{pLH})}{2} \tag{4.2}$$

The values of τ_{pHL} and τ_{pLH} are explained in Figure 4.1 and they are expressed as follows:

$$\tau_{pHL} = \frac{C_{load}}{k_n(V_{DD} + V_{THn})}\left[\frac{2V_{THn}}{V_{DD} - V_{THn}} + ln\left(\frac{4(V_{DD} - V_{THn})}{V_{DD}} - 1\right)\right] \tag{4.3}$$

$$\tau_{pLH} = \frac{C_{load}}{k_p(V_{DD} + |V_{THp}|)}\left[\frac{2|V_{THp}|}{V_{DD} - |V_{THp}|} + \ln\left(\frac{4(V_{DD} - |V_{THp}|)}{V_{DD}} - 1\right)\right] \tag{4.4}$$

C_{load} refers to the total capacitive load of the inverter. It is noteworthy that $k = \frac{\mu C_{ox} W}{L}$; k_p and k_n refer to the k values for the *p*- and *n*-channel FETs. As shown in equation (4.1), a decrease in n results in an increase in f_{osc}. However, a decrease in n may not be realistic because n = 5 appears to be the smallest number of inverters in the ring oscillator [71].

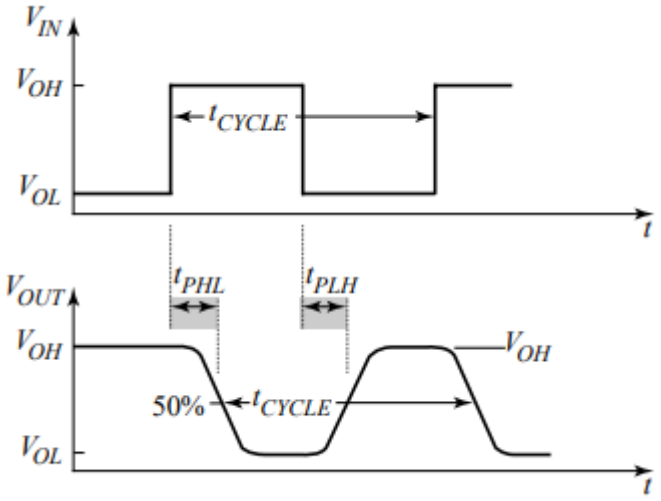


Figure 4.1 *- The top graph shows the input voltage of a CMOS inverter. The graph below shows the output voltage of a CMOS inverter. The two times* τ_{pHL} *and* τ_{pLH} *are shown*

As shown in equations (4.1) – (4.4), a smaller L should provide a smaller through a larger k_p and k_n. Consequently, a smaller $< \tau_p >$ results in a larger f_{osc}. It is noteworthy that a larger W (= 500 or 1000 μm) in the PTCDI-C8 thinfilm FET than that (W = 200 or 300 μm) in the *p*-channel FET was used in the ring oscillator such that the small μ value obtained in the *n*-channel PTCDI-C8 FET was compensated in $k_n = \frac{\mu_n C_{ox} W_n}{L_n}$. To summarize, the fabrication of the ring oscillator with a smaller L (i.e., fabrication of microscale ring oscillator) is significant for increasing the value of f_{osc}. Furthermore, a larger value of μ must be realized in *n*-channel FETs.

4.1 Characteristics of organic ring oscillators

A SiO_2/Si substrate was employed to prepare the ring oscillator. Before the fabrication of the FET device, the SiO_2/Si substrate was cleaned according to the procedure described elsewhere.26 The structures of organic molecules employed for the ring oscillator, [6]pehanacene, $(C_{14}H_{29})_2$-picene, and PTCDI-C8 are shown in Figure 4.2(a). The equivalent circuit of the five-step ring oscillator is shown in Figure 4.2(b). The ring oscillator was fabricated according to the procedure shown in Figure 4.2(c).

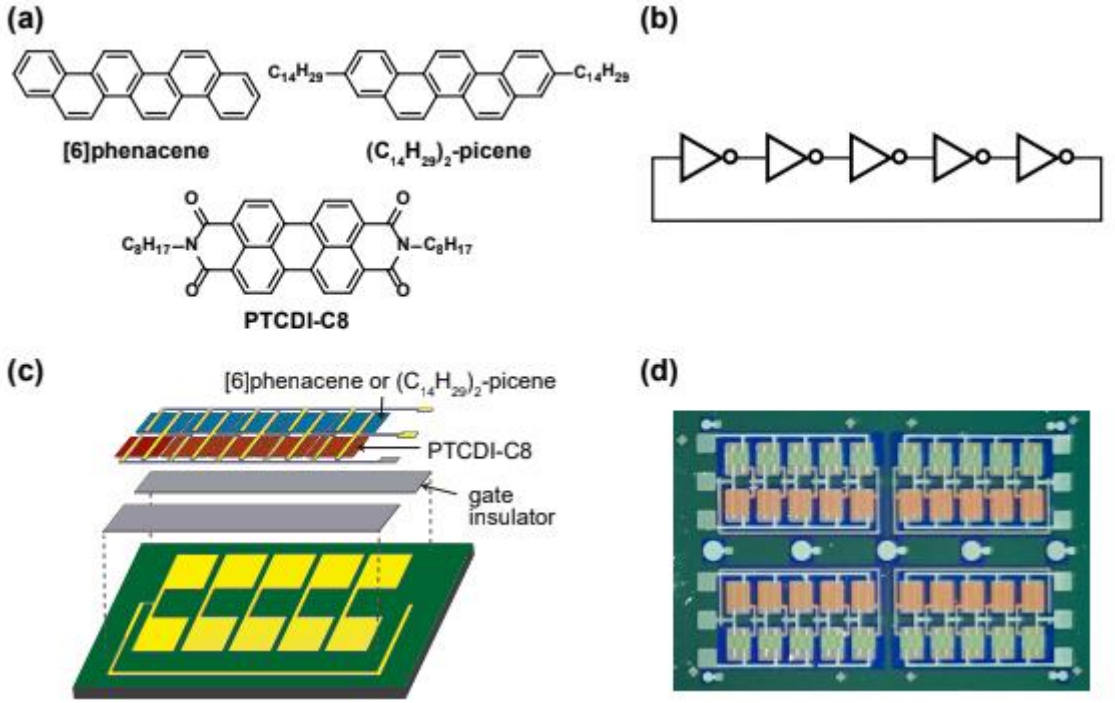


Figure 4.2 *- a) Molecular structure of organic molecules used in this study. b) Ring oscillator schematic. c) Organic ring oscillator layers. d) Picture of 4 organic ring oscillators*

First, the bottom electrodes were prepared on the SiO_2/Si substrate, which become the input electrodes for operating the FETs constituting each inverter. Next, a 600 nm thick parylene or 320 nm thick ZrO_2 gate dielectric was formed on the bottom electrodes. The ZrO_2 thin film was prepared by electron beam deposition. The gate dielectric was not formed in the central area to establish contacts between the output and input electrodes in each inverter. Subsequently, active layers were prepared by the thermal deposition of organic materials under

a vacuum of 10^{-7} Torr for *p*-channel and *n*-channel FET operations; either [6]phenacene or $(C_{14}H_{29})_2$-picene was used for the *p*-channel active layer, while PTCDI-C8 for the *n*-channel active layer. The thickness of the active layer was 60 nm. Finally, the top electrodes were fabricated for voltage application (V_{DD}), ground (*GND*), and detection of output voltage (V_{out}). All electrodes were formed by the thermal deposition of gold (Au) under a vacuum of 10^{-7} Torr, and the Au layer was 100 nm thick for the bottom electrodes, and 150 nm for the top electrodes. Furthermore, 5 nm thick chromium (Cr) was inserted between the bottom electrode and SiO_2/Si substrate to increase the adhesion, while a 3 nm thick 7,7,8,8-teracyano-quinodimethane was inserted between the active layer and top electrodes to reduce the contact resistance. A photograph of the ring oscillator prepared is shown in Figure 4.2(d). In this study, the ring oscillators were prepared for active layers using $(C_{14}H_{29})_2$-picene and PTCDI-C8 FETs, as well as [6]phenacene and PTCDI-C8 FETs, where a parylene gate dielectric was used. Moreover, the ring oscillator was fabricated using [6]phenacene and PTCDI-C8 FETs, as well as ZrO_2 gate dielectric to reduce the operation voltage.

The channel length (I) of the ring oscillator comprising [6]phenacene and PTCDI-C8 FETs with parylene gate dielectrics was 200 μm, while the values of channel width (*W*) were 200 μm for [6]phenacene FET and 500 μm for PTCDI-C8 FETs in this ring oscillator. The *L* value of the ring oscillator comprising $(C_{14}H_{29})_2$-picene and PTCDI-C8 FETs with parylene gate dielectrics was 300 μm, while the *W* values were 500 μm for $(C_{14}H_{29})_2$-picene FET and 1000 μm for PTCDI-C8 FETs in the ring oscillator. Moreover, the *L* of the ring oscillator comprising [6]phenacene and PTCDI-C8 FETs with ZrO*2* gate dielectrics was 300 μm, while the values of *W* were 500 μm for [6]phenacene FET and 1000 μm for PTCDI-C8 FETs in this ring oscillator.

The capacitance per area for the parylene gate dielectric, C_0, was determined experimentally to be 4.57 nF cm^{-2} in the ring oscillator comprising [6]phenacene/PTCDIC8 FETs and 6.15 nF cm^{-2} in that comprising $(C_{14}H_{29})_2$-

picene/PTCDI-C8 FETs. The C_0 value for ZrO2 was experimentally determined to be 30.9 nF cm^{-2} in the ring oscillator comprising [6]phenacene/PTCDI-C8 FETs. The operation properties of each FET device and inverter constituting the ring oscillator were measured in two-terminal measurement modes at room temperature. The operation properties were recorded using an Agilent B1500A semiconductor parametric analyzer in an Ar-filled glove box.

4.2 [6]phenacene/PTCDI-C8 organic ring oscillator with parylene gate dielectric

In this section are described the properties of organic ring oscillators made by using [6]phenacene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs, formed on SiO_2/Si substrate.

4.2.1 Properties of [6]phenacene/PTCDI-C8 FETs

Figures 4.3(a) and (b) show the transfer and output characteristics of the [6]phenacene thin-film FET, which constitutes the *p*-channel part of one CMOS inverter in the ring oscillator; the *n*-channel part of the inverter is composed of PTCDI-C8 FET. The ring oscillator comprises five inverters, in which a 600-nm-thick parylene layer was used for the gate dielectric. The ring oscillator provides an f_{osc} value of 26 Hz, which will be described later. As shown in Figures 4.3(a) and (b), *p*-channel FET characteristics were observed for the [6]phenacene FET, and weak *n*-channel FET properties were observed as well, indicating ambipolar properties. The characteristics of the [6]phenacene thin-film FET were affected by the PTCDI-C8 thin-film FET, which typically exhibits *n*-channel FET characteristics. Moreover, as shown in Figures 4.3(c) and (d), the PTCDI-C8 thin-film FET showed not only *n*-channel FET characteristics, but also weak *p*-channel

characteristics, i.e., weak ambipolar characteristics were observed as well, as in the [6]phenacene FET. Ambipolar characteristics were observed because another FET was operating below the absolute threshold voltage $|V_{th}|$ for each FET.

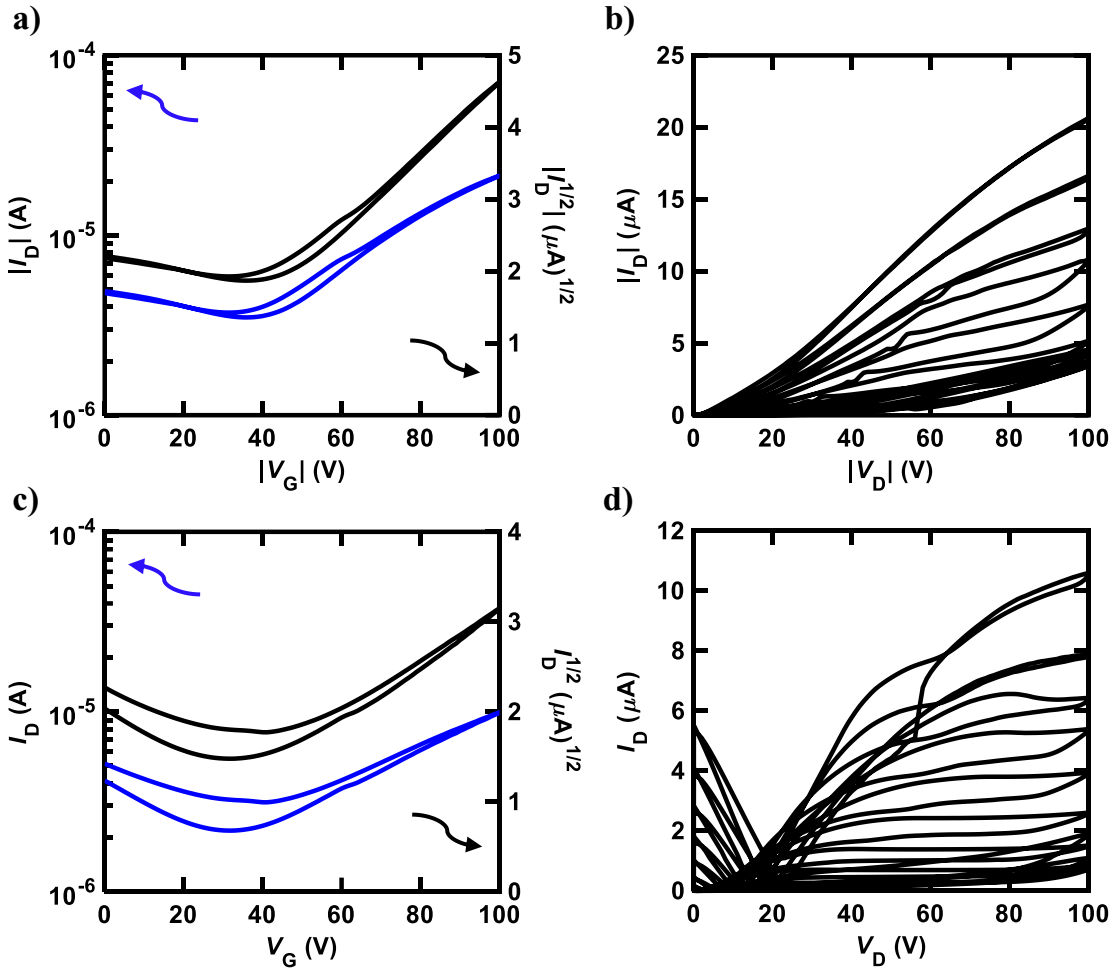


Figure 4.3 *a) Transfer and b) output curves of [6]phenacene thin-film FET used as p-channel FET; c) transfer and d) output curves of PTCDI-C8 thin fil FET used as n-channel FET*

The FET parameters of the [6]phenacene and PTCDI-C8 thin-film FETs in the inverters constituting the ring oscillator (f_{osc} = 26 Hz) fabricated in this study are listed in Table 4.1. The average values of μ and V_{th} (<μ> and <V_{th}>) were 8(4) × 10^{-1} $cm^2 V^{-1} s^{-1}$ and -2(3) × 10 V for the [6]phenacene thin-film FET, respectively.

Because of the ambipolar FET properties, the <μ> and <V_{th}> were subpar, *i.e.*, low μ and high <$|V_{th}|$> were obtained, in comparison with those recorded for the normal [6]phenacene thin-film FET.

In particular, the average on–off ratio (<on–off ratio>) was low, as shown in Table 4.1. The high *S* factor (<*S*>) was owing to the ambipolar properties. The values of <μ> and <V_{th}> were 2.0(4) × 10^{-1} cm^2 V^{-1} s^{-1} and 3(7) V for PTCDI-C8 thin-film FET, respectively; the μ value was much lower than that in the FET using a PTCDI-C8 thin film formed on pentacene, as reported recently.31 The values of <on–off ratio> and <*S*> were subpar because of the ambipolar properties observed in a series connection of CMOS inverters composed of *p*-channel and *n*-channel FETs. To summarize, the relatively low FET properties recorded in this study were not due to the intrinsic nature of materials employed, but the electrical series connections of inverters.

Table 4.1 *FET parameters of [6]phenacene and PTCDI-C8 thin-film FETs*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)
#1	8.1×10^{-1}	7.0×10^{1}	2686.42	2.7×10^{1}
#2	8.1×10^{-1}	3.1×10^{1}	2.71	8.2×10^{1}
#3	1.19	1.1×10^{1}	6.12	6.1×10^{1}
#4	2.7×10^{-1}	-1.7×10^{1}	2.44	1.2×10^{2}
#5	1.16	1.4×10^{1}	5.71	5.9×10^{1}

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)
#1	2.33×10^{-1}	8.7	4.8×10^{1}	1.0×10^{1}
#2	1.69×10^{-1}	-1.5	3.2	9.7×10^{1}
#3	1.50×10^{-1}	-7.7	3.1	9.9×10^{1}
#4	1.96×10^{-1}	6.1	4.8	8.0×10^{1}
#5	2.27×10^{-1}	9.9	4.7	8.0×10^{1}

4.2.2 Properties of [6]phenacene/PTCDI-C8 CMOS inverters

Figure 4.4 shows plots of V_{out}–V_{in} (inverter characteristics) and $|\mathrm{d}V_{out}/\mathrm{d}V_{in}|$ – V_{in} (gain plot) for one CMOS inverter comprising [6]phenacene and PTCDI-C8

thin-film FETs, which constitutes the ring oscillator with an f_{osc} of 26 Hz. The inverter contains the [6]phenacene and PTCDI-C8 thin-film FETs described in Section 4.2.1. Clear inverter properties were observed in the plot shown in Figure 4.4. The V_{DD} was 100 V. As shown in Figure 4.3, the V_{in} (59.4 V for the forward measurement and 47.0 V for the reverse measurement) providing half the maximum value of V_{out} (called "logic threshold voltage (V_{TC})") is slightly deviated from the ideal value of $V_{DD}/2 = 50$ V. The gain plot of the CMOS inverter with [6]phenacene and PTCDI-C8 thin-film FETs is shown in Figure 4.4, which was obtained from the first derivative of the V_{out}–V_{in} plot. The gain of the CMOS inverter above was evaluated to be 285.8 for the forward measurement and 71.6 for the reverse measurement.

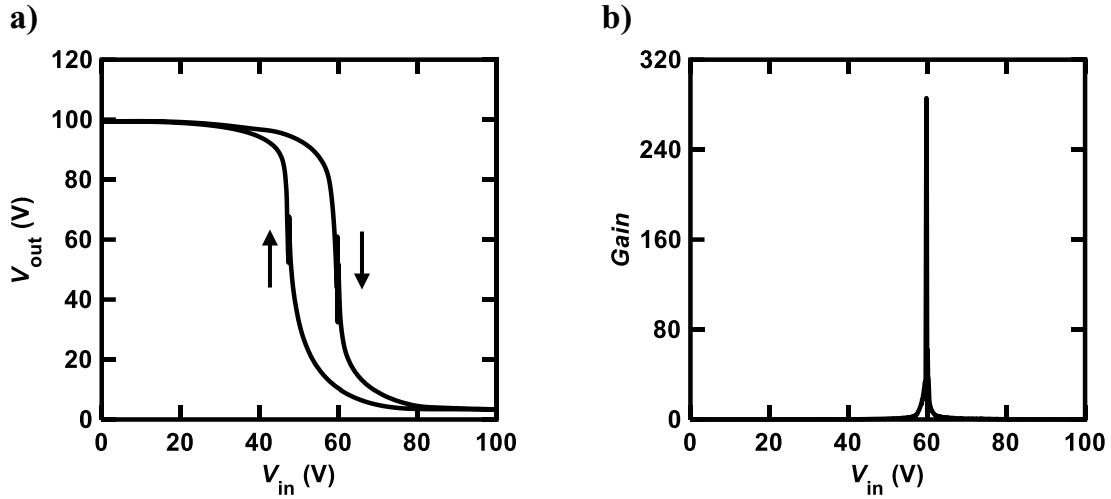


Figure 4.4 *- a) Vout-Vin curve of a [6]phenacene/PTCDI-C8 inverter. b) Gain curve of a [6]phenacene/PTCDI-C8 inverter*

The V_{TC} value of the CMOS inverter circuit is given by equation (3.1):

$$V_{\mathrm{TC}} = \frac{V_{\mathrm{DD}} - \left|V_{\mathrm{THp}}\right| + V_{\mathrm{THn}}\sqrt{k_{\mathrm{R}}}}{1 + \sqrt{k_{\mathrm{R}}}} \tag{3.1}$$

By substituting the FET parameters obtained in Section 3-1 into equation (3.1), we evaluated the V_{TC} for the CMOS inverter above and obtained a value of 54.2

V. This VTC value is consistent with the observed value (V_{TC} = 59.4 V and V_{TC} = 47.0 V), which indicates the effectiveness of the above equation and the reliability of the FET parameters in Section 4.2.1. The values of gain and V_{TC} for all inverters constituting the ring oscillator are listed in Table 4.2; the plots shown in Figure 4.4 are obtained using inverter device (#3) in Table 4.2.

Table 4.3 *[6]phenacene / PTCDI-C8 inverter parameters*

device	V_{TC} (V)	*Gain*
#1	55.9	32.9
#2	37.7	67.8
#3	59.4	285.8
#4	58.2	181.4
#5	54.9	146.6

4.2.3 Properties of [6]phenacene/PTCDI-C8 ring oscillators

Figure 4.5 (a) shows the $V_{out} - t$ plot for the ring oscillator comprising five CMOS inverters; each inverter was fabricated using a [6]phenacene thin-film FET for a *p*-channel operation and a PTCDI-C8 thin-film FET for an *n*-channel operation. Furthermore, a 600 nm thick parylene film was used for the gate dielectric in the ring oscillator. The channel length and width for *p*-channel FETs was 200 μm and 300 μm, respectively. The channel length and width for *n*-channel FETs was 200 μm and 500 μm, respectively.

Table 4.4 *[6]phenacene / PTCDI-C8 ring oscillators*

device	V_{DD} (V)	f_{osc} (Hz)	$L_{n,p}$ (μm)	W_n (μm)	W_p (μm)
#1	100	0.9	300	1000	500
#2	100	2	300	1000	500
#3	100	0.6	200	1000	500
#4	100	26	200	500	300

As shown in Figure 4.5 (a), the value of the operation frequency, f_{osc} was 26 Hz when V_{DD} was 100 V. This is the first demonstrated decent operation of a ring oscillator using phenacene molecules, although the f_{osc} values of other devices has been reported in Table 4.4. As shown in Figure 4.5 (a), the f_{osc} was 26 Hz when the applied V_{DD} was 100 V. The ring oscillator was operated continuously for 2 hours, and then the $V_{out} - t$ plot was recorded (Figure 4.5 (b)), indicating a 16 Hz operation in the ring oscillator.

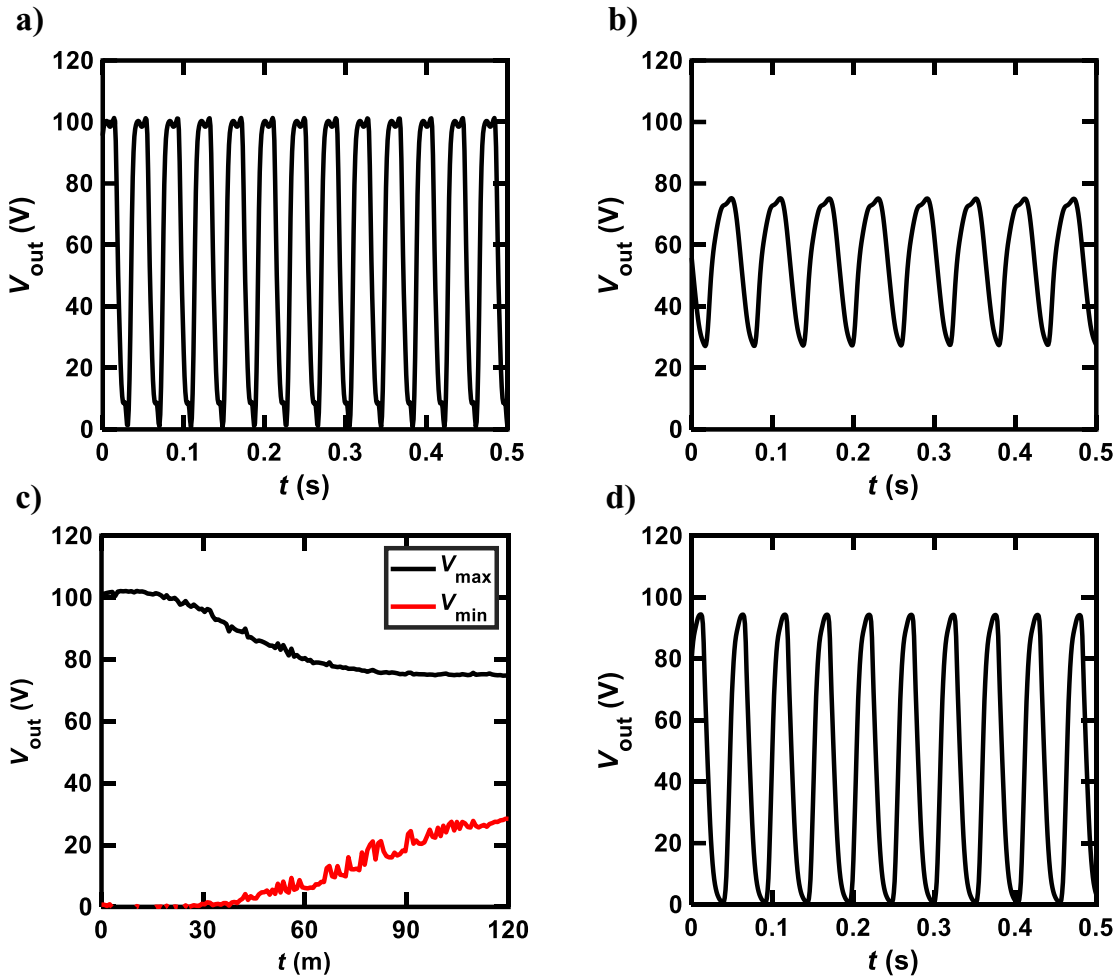


Figure 4.5 *- a) [6]phenacene/PTCDI-C8 ring oscillator V_{out}-V_{in} curve (f_{osc} = 26 Hz). b) The same ring oscillator, after 2 hours, where a V_{dd} = 100V was applied (f_{osc} = 16 Hz). c) V_{max} and V_{min} curves during 2 hours where V_{dd} = 100V was applied. d) The same oscillator was measured after 2 months and gives an oscillation frequency f_{osc} = 19 Hz.*

Namely, the value of f_{osc} decreased from 26 to 16 Hz by a continuous application of V_{DD} = 100 V. We stopped the operation of the ring oscillator and stored the ring oscillator without any V_{DD} for two months. After two months, we

recorded the $V_{out} - t$ plot (Figure 4.5(d)), which showed an f_{osc} value of 19 Hz, and a V_{out} amplitude of 90 V. Therefore, the oscillation performance was recovered by not applying V_{DD} for two months.

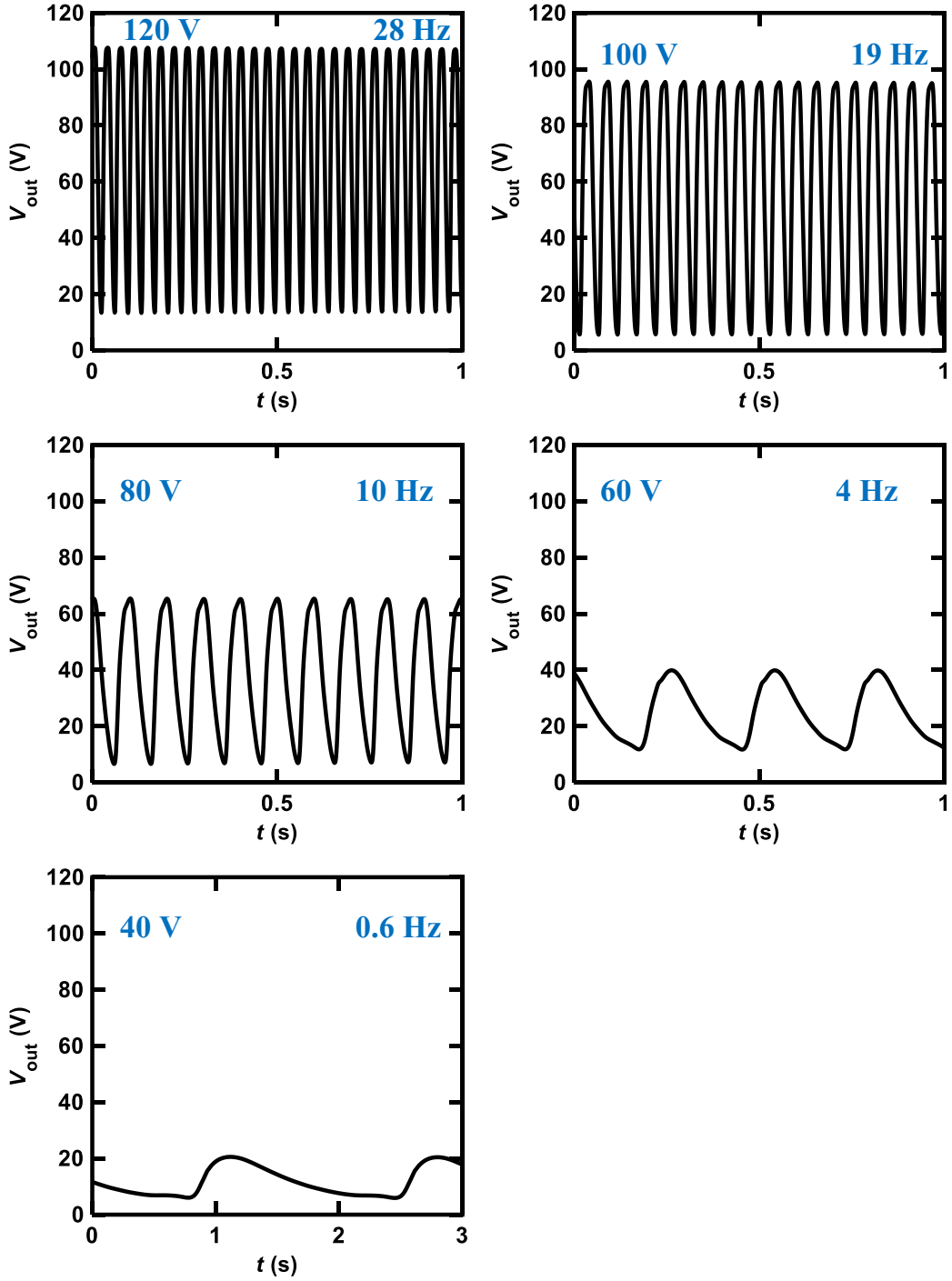


Figure 4.6 *- Oscillation frequency (f_{osc}) of [6]phenacene/PTCDI-C8 ring oscillator at different V_{DD} voltages*

After 2 months, we changed the V_{DD} value applied for the ring oscillator to verify the operation properties. Figure 4.6 shows the $V_{out} - t$ plots for the ring oscillator composed of five inverters using [6]phenacene and PTCDI-C8 FETs, with the parylene gate dielectric measured at different V_{DD}. When V_{DD} was decreased from 120 to 40 V, the f_{osc} and amplitude of V_{out} decreased gradually. Namely, the fosc was 28 Hz for V_{DD} = 120 V, and 10 Hz for V_{DD} = 80 V. Below V_{DD} = 40V, oscillations were not observed. Therefore, it was found that the threshold V_{DD} for oscillation was 40 V for this ring oscillator.

4.3 $(C_{14}H_{29})_2$-picene/PTCDI-C8 organic ring oscillator with parylene gate dielectric

In this section are described the properties of organic ring oscillators made by using $(C_{14}H_{29})_2$-picene as active layer for *p*-channel FETs and PTCDI-C8 for *n*-channel FETs, formed on SiO_2/Si substrate.

4.3.1 Properties of $(C_{14}H_{29})_2$-picene/PTCDI-C8 FETs

Figures 4.7 (a) and (b) show the transfer and output characteristics of the $(C_{14}H_{29})_2$-picene thin-film FET, which constitutes the *p*-channel part of one CMOS inverter in the ring oscillator, providing an f_{osc} value of 21 Hz. PTCDI-C8 was employed as the active layer of the *n*-channel part.

As shown in Figures 4.7(a) and (b), *p*-channel FET characteristics were observed for the $(C_{14}H_{29})_2$-picene FET, together with clear *n*-channel FET characteristics, indicating ambipolar properties. Therefore, the operation of the $(C_{14}H_{29})_2$-picene thin-film FET was affected by the PTCDI-C8 thin-film FET.

As shown in Figures 4.7 (c) and (d), the PTCDI-C8 thin-film FET showed not only *n*-channel FET characteristics, but also *p*-channel characteristics.

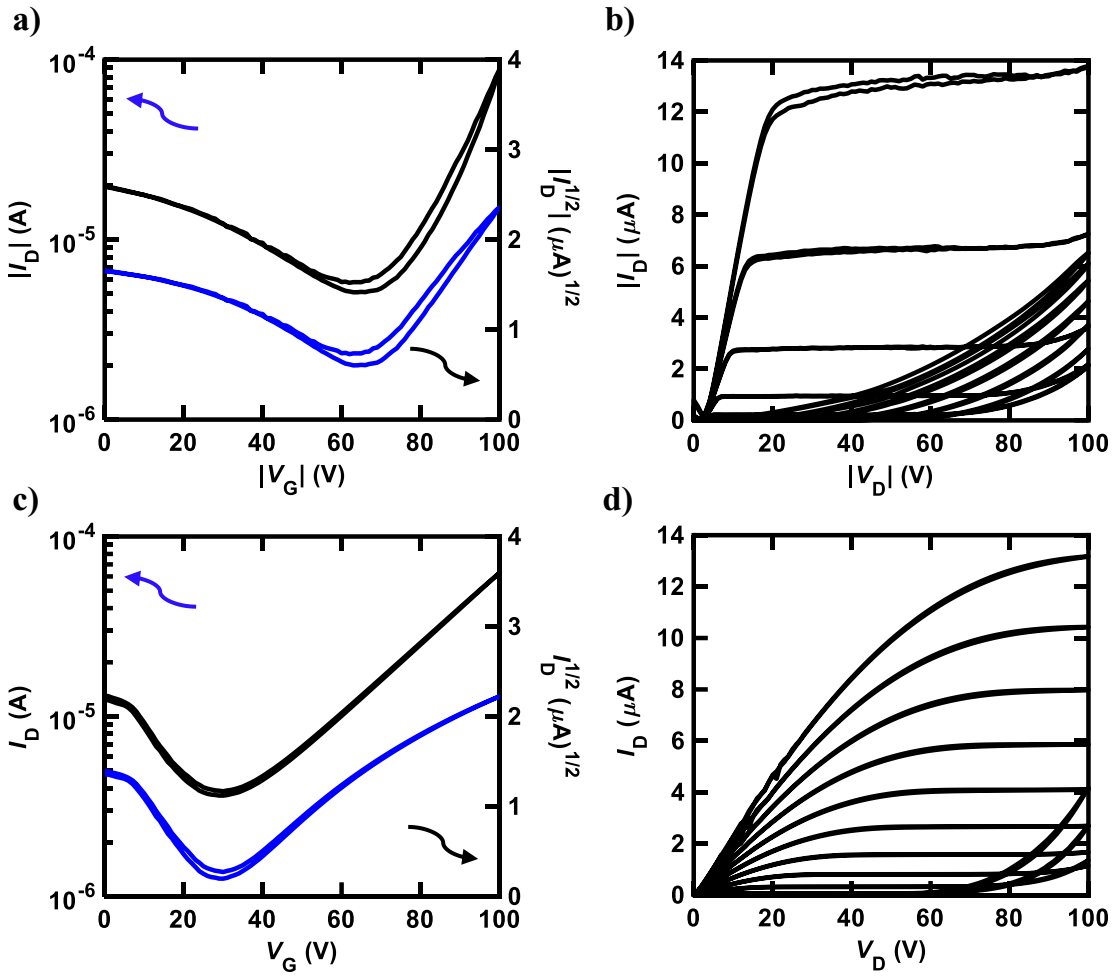


Figure 4.7 *- a) Transfer and b) output curves of $(C_{14}H_{29})_2$-picene thin-film FET used as p-channel FET; c) transfer and d) output curves of PTCDI-C8 thin-film FET used as n-channel FET*

Therefore, the ambipolar FET characteristics in the $(C_{14}H_{29})_2$-picene/PTCDI-C8 inverter are clearer than those discovered in the CMOS inverter with [6]phenacene and PTCDI-C8. In addition, a small hysteresis was observed in the forward and reverse transfer curves, which probably originates from the bias stress effect.

All FET parameters in the $(C_{14}H_{29})_2$-picene thin-film and PTCDI-C8 thin-film FETs in the CMOS inverters constituting the ring oscillator (f_{osc} = 21 Hz) fabricated in this study are listed in Table 4.5. The average values of μ and V_{th} ($<\mu>$ and $<V_{th}>$) were 1.4(7) $cm^2V^{-1}s^{-1}$ and -5.9(9) × 10 V for the $(C_{14}H_{29})_2$-picene

thin-film FET, respectively. The low and high were due to the ambipolar properties observed in the series connection of CMOS inverters.

Table 4.5 *FET parameters of $(C_{14}H_{29})_2$-picene and PTCDI-C8 thin-film FETs*

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)
#1	1.85	6.0×10^{1}	6.6	3.60×10^{1}
#2	2.40×10^{-1}	4.4×10^{1}	6.8	5.24×10^{1}
#3	1.73	6.3×10^{1}	9.8	2.99×10^{1}
#4	1.90	6.4×10^{1}	7.0	3.37×10^{1}
#5	1.19	6.6×10^{1}	5.4	3.13×10^{1}

device	μ ($cm^2V^{-1}s^{-1}$)	$\lvert V_{th}\rvert$ (V)	*ON/OFF*	*S* (V/decade)
#1	1.54×10^{-1}	9.49	1.03×10^{1}	5.13×10^{1}
#2	3.10×10^{-2}	9.74	8.29	4.92×10^{1}
#3	1.53×10^{-1}	8.51	1.82×10^{1}	5.08×10^{1}
#4	1.53×10^{-1}	9.39	1.21×10^{1}	5.00×10^{1}
#5	1.52×10^{-1}	8.60	1.30×10^{1}	4.66×10^{1}

The values of and were $1.3(5) \times 10^{-1}$ $cm^2V^{-1}s^{-1}$ and 9.2(6) V for the PTCDI-C8 thin-film FET, respectively. Similarly, the low values of and were likely due to the effects of ambipolar properties observed in the series connection of CMOS inverters.

4.3.2 Properties of $(C_{14}H_{29})_2$-picene/PTCDI-C8 CMOS inverters

Figure 4.8 shows plots of $V_{out} - V_{in}$ and $|dV_{out}/dV_{in}| - V_{in}$ for one CMOS inverter comprising $(C_{14}H_{29})_2$-picene and PTCDI-C8 thin-film FETs, which constitutes the ring oscillator with an f_{osc} of 21 Hz. The inverter is composed of the $(C_{14}H_{29})_2$-picene and PTCDI-C8 thin-film FETs evaluated in Section 4.3.1. Clear inverter properties were observed in the $V_{out} - V_{in}$ plot shown in Figure 4.8; the V_{DD} was

100 V. As shown in Figure 4.8, the observed value of V_{TC} (38.9 V for the forward measurement and 33.9 V for the reverse measurement) deviated from the value of $V_{DD}/2$ = 50 V. The gain plot obtained from the first derivative of the $V_{out} - V_{in}$ plot (Figure 4.8) for the CMOS inverter with $(C_{14}H_{29})_2$-picene and PTCDI-C8 thin-film FETs is shown in Figure 4.8. The gain of the above CMOS inverter was evaluated to be 61.8 for the forward measurement and 90.8 for the reverse measurement.

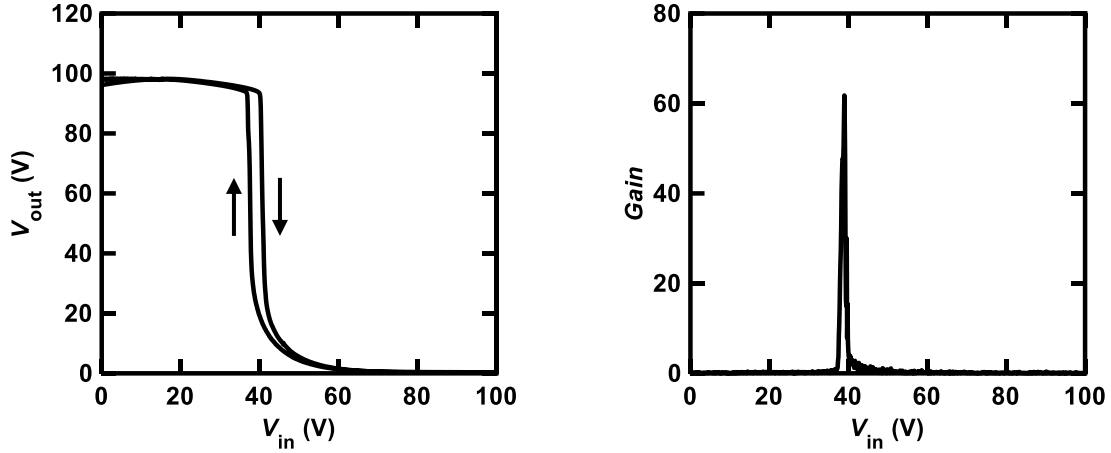


Figure 4.8 *- a) Vout-Vin curve of a $(C_{14}H_{29})_2$-picene/PTCDI-C8 inverter. b) Gain curve of a $(C_{14}H_{29})_2$-picene/PTCDI-C8 inverter*

measurement of the inverter properties, which may suppress the gain of each inverter. Using equation (2), we evaluated the theoretical value of V_{TC} for the CMOS inverter and obtained a value of 31.2 V. This V_{TC} value is consistent with the observed value (V_{TC} = 38.9 V for the forward measurement and 33.9 V for the reverse measurement), which also indicates the effectiveness of the equation 3.1 and the reliability of the FET parameters in Section 4.3.1. The values of gain and V_{TC} for all inverters constituting the ring oscillator are listed in Table 4.6; the plots shown in Figure 4.8 are obtained using the inverter device (#1).

Table 4.6 ($C_{14}H_{29})_2$-picene*/PTCDI-C8 inverter parameters*

device	V_{TC} (V)	*Gain*
#1	38.9	61.8
#2	38.8	54.1
#3	41.1	50.9
#4	38.6	56.5
#5	36.6	47.1

4.3.3 Properties of $(C_{14}H_{29})_2$-picene/PTCDI-C8 ring oscillators

Figure 4.9 shows the $V_{out} - t$ plot for a ring oscillator comprising five CMOS inverters; each inverter was fabricated using a $(C_{14}H_{29})_2$-picene thin-film FET for a *p*-channel operation and a PTCDI-C8 thin-film FET for an *n*-channel operation. Furthermore, a 600 nm thick parylene film was used for the gate dielectric in this ring oscillator. The channel length and width for *p*-channel FETs was 200 μm and 500 μm, respectively. The channel length and width for *n*-channel FETs was 200 μm and 1000 μm, respectively. As shown in Figure 4.9 the value of f_{osc} was 21 Hz when a V_{DD} of 100 V was applied. Therefore, the clear operation of the ring oscillator was confirmed when using $(C_{14}H_{29})_2$-picene/PTCDI-C8 FETs, indicating the possibility of applying the above FETs for RFID devices.

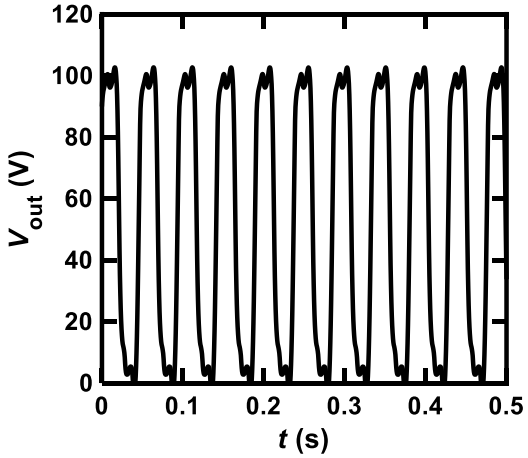


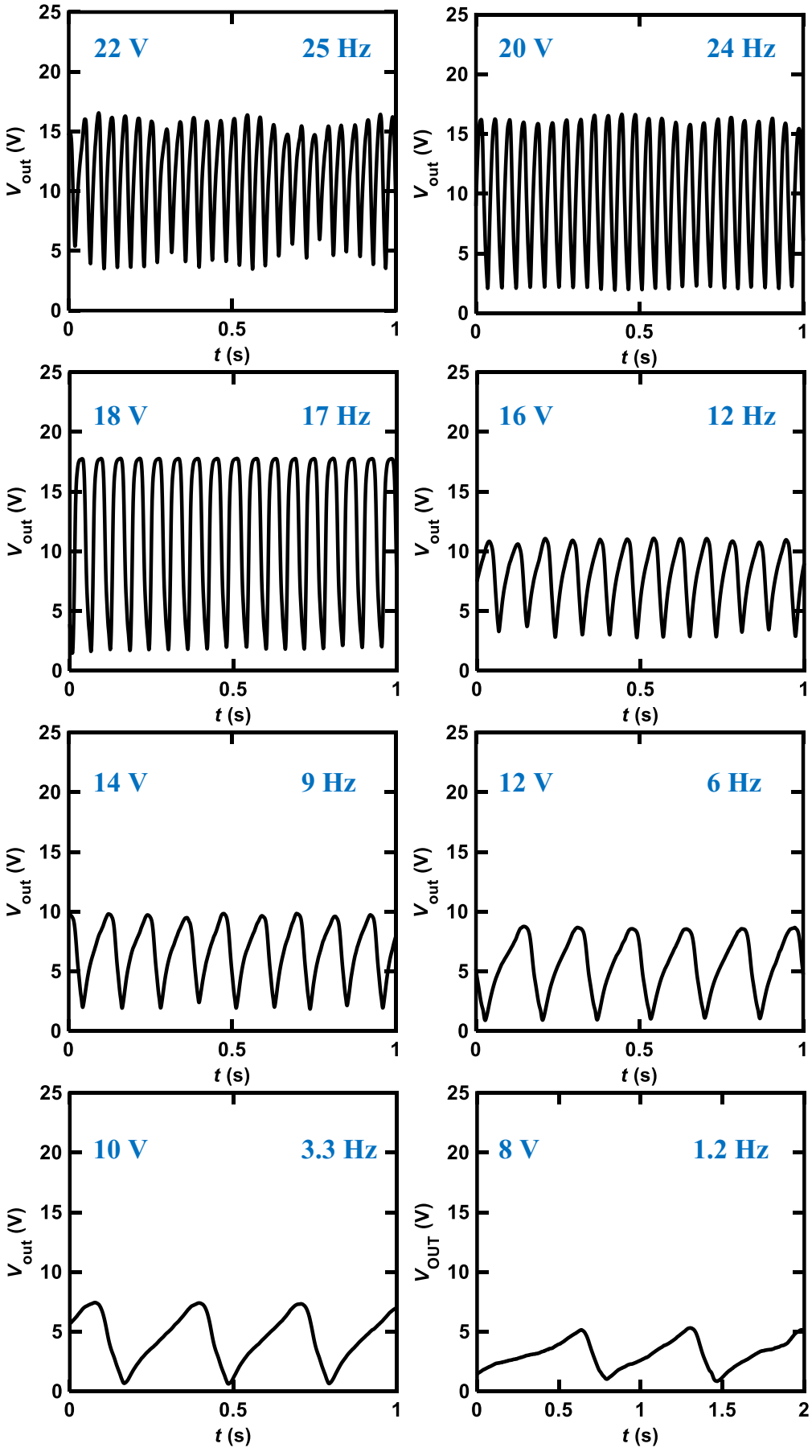
Figure 4.9 *- $(C_{14}H_{29})_2$-picene/PTCDI-C8 ring oscillator Vout-Vin curve (fosc = 21 Hz).*

We report another ring oscillator made by $(C_{14}H_{29})_2$-picene/PTCDI-C8 FETs that has f_{osc} equal to 18 Hz. The dimension of the channel (length and width) was the same as the previous one: 200 μm/500 μm for *p*-channel FETs and 200 μm/1000 μm for *n*-channel FETs.

4.4 [6]phenacene/PTCDI-C8 organic ring oscillator with ZrO_2 gate dielectric

We attempted to fabricate a ring oscillator incorporating five inverters composed of [6]phenacene/PTCDI-C8 FETs with a ZrO_2 gate dielectric to realize a low voltage operation. The $V_{out} - t$ plot of the ring oscillator is shown in Figure 4.10. A V_{DD} of 20 V was applied for this ring oscillator, providing a 24 Hz oscillation. The channel length and width for *p*-channel FETs was 200 μm and 200 μm, respectively. The channel length and width for *n*-channel FETs was 200 μm and 500 μm, respectively. This device performance is comparable to those of the ring oscillators above using parylene gate.

Figure 4.10 shows the $V_{out} - t$ plots for the ring oscillator composed of five inverters using [6]phenacene and PTCDI-C8 FETs with ZrO_2 gate dielectrics measured at different V_{DD}. By decreasing V_{DD} from 22 to 8 V, the f_{osc} decreased gradually. Namely, the f_{osc} was 25 Hz for V_{DD} = 22 V and 8.8 Hz for V_{DD} = 14 V. Below V_{DD} = 8 V, oscillations were not observed. Thus, the threshold V_{DD} for the oscillation of this ring oscillator was 8 V, showing the operation of a ring oscillator at a lower voltage than that (threshold V_{DD} of 40 V) for the previous ring oscillator (Figure 4.6). Namely, the ZrO_2 gate dielectric used in the ring oscillator resulted in a low-voltage operation.


22 V
25 Hz
20 V
24 Hz
18 V
17 Hz
16 V
12 Hz
14 V
9 Hz
12 V
6 Hz
10 V
3.3 Hz
8 V
1.2 Hz
V_{out} (V)
V_{OUT} (V)
t (s)

Conclusions

The organic FET has promising applications toward human-compatible devices such as electronic skin and biomedical sensor as well as ubiquitous devices such as flexible display, electronic paper and information tag. However, there are still many problems to be solved for future practical application, *i.e.*, the μ value, operation voltage, durability and stability are inferior to those of inorganic MOS FET. Furthermore, the advantages in organic FET such as flexibility and ease of design must be further advanced.

In this study, the successful operation of a ring oscillator composed of five CMOS inverters using phenacene and PTCDI-C8 thin-film FETs was demonstrated. An f_{osc} value exceeding 20 Hz was stably observed using a [6]phenacene or $(C_{14}H_{29})_2$-picene thin-film FET for a *p*-channel operation and a PTCDI-C8 thin-film FET for an *n*-channel operation. A parylene gate dielectric was used for the ring oscillator. Moreover, the ring oscillator using CMOS inverters composed of [6]phenacene and PTCDI-C8 FETs with ZrO_2 showed a low-voltage operation. The value of f_{osc} obtained was the same as that using the parylene gate dielectric. The duration experiment of the ring oscillator clarified the presence of the bias stress effect in the ring oscillator, *i.e.*, the f_{osc} and V_{out} amplitude decreased significantly. However, the performance of the ring oscillator was recovered by storing the device without applying a V_{DD} for two months. The successful decent operation of the ring oscillator demonstrated a potential application of phenacene molecules toward logic gate circuits, and the fabrication process of the ring oscillator was shown clearly in this study.

Therefore, this is of significance as the initial stage of the development of the high-performance logic gate circuits using phenacene molecules even if the oscillation frequency is still low. In other words, this study can serve as a basis for the fabrication of RFIDs using phenacene molecules.

Bibliography

[1] J. E. Lilienfeld, “Method and apparatus for controlling electric current,” *Patent US1745175A,* 1930.

[2] J. E. Lilienfeld, “Device for controlling electric current,” *Patent US1900018A,* 1933.

[3] W. H. Brattain and J. Bardeen, “Three-electrode circuit element utilizing semiconductive materials,” *Patent US2524035A,* 1950.

[4] H. Welker and H. F. Mataré, “Crystal device for controlling electric currents by means on a solid semiconductor,” *Patent US2673948A,* 1954.

[5] D. Kahng, “Electric field controlled semiconductor device,” *Patent US3102230,* 1963.

[6] M. M. Atalla, “Junction formation by thermal oxidation of semiconductive material,” *Patent US2953486A,* 1960.

[7] D. Kahng, “Silicon-silicon dioxide surface devices,” *IRE-AIEE Solid State Device Research Conference,* 1960.

[8] C. T. Sah, “A New Semiconductor Tetrode-The Surface-Potential Controlled Transistor,” *Proceedings of the IRE. 49 (11),* p. 1623–1634, 1961.

[9] F. M. Wanlass and C. T. Sah, “Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes,” *International Solid State Circuits Conference Digest of Technical Papers,* pp. 32-33, 1963.

[10] F. M. Wanlass, “Low Stand-By Power Complementary Field Effect Circuitry,” *Patent US3356858A,* 1967.

[11] R. Ahrons and J. B. M. Mitchell, “MOS micropower complementary transistor logic,” *IEEE International Solid-State Circuits Conference. Digest of Technical Papers. 1965 Vol.,* pp. 80-81, 1965.

[12] C. Hanchett, S. Katz and A. K. Yung, “Complementary MOS Memory Arrays,” *Government Microcircuits Applications Conference, Reprinted as RCA Publication No. ST-3814,* 1968.

[13] Y. Suzuki, K. Odagawa and T. Abe, “Clocked CMOS calculator circuitry,” *IEEE Journal of Solid-State Circuits,* vol. 8, no. 6, pp. 462-469, 1973.

[14] T. Masuhara, O. Minato, T. Sasaki, Y. Sakai, M. Kubo and T. Yasui, “A high-speed, low-power Hi-CMOS 4K static RAM,” *EEE International Solid-State Circuits Conference. Digest of Technical Papers 1978,* vol. XXI, no. 110-111, 1978.

[15] K. Kuhn, High Mobility Materials, Woodhead Publishing, 2018.

[16] A. Bernanose, M. Comte and P. Vouaux, “A new method of light emission by certain organic compounds,” *J. Chim. Phys.,* vol. 50, pp. 64-68, 1953.

[17] A. Bernanose and P. Vouaux, “Organic electroluminescence type of emission,” *J. Chim. Phys.,* vol. 50, pp. 261-263, 1953.

[18] A. Bernanose, “The mechanism of organic electroluminescence,” *J. Chim. Phys.,* vol. 52, pp. 396-400, 1955.

[19] A. Tsumura, H. Koezuka and T. Ando, “Macromolecular electronic device: field-effect transistor with a polythiophene thin film,” *Applied Physics Letters,* vol. 49, no. 18, pp. 1210-1212, 1986.

[20] A.Tsumura, H.Koezuka and T.Ando, “Field-effect transistor with polythiophene thin film,” *Synthetic Metals,* vol. 18, no. 1-3, pp. 699-704, 1987.

[21] A. Assadi, C. Svensson, M. Willander and O. Inganas, “Field-effect mobility of poly(3-hexylthiophene),” *Applied Physics Letters,* vol. 53, pp. 195-197, 1988.

[22] G. Horowitz, “A field-effect transistor based on conjugated alpha-sexithienyl,” *Solid State Communications,* vol. 72, pp. 381-384, 1989.

[23] G. Horowitz, X. Peng, D. Fichou and F. Garnier, “Organic thin-film transistors,” *Journal of Molecular,* vol. 7, pp. 85-89, 1991.

[24] G. Horowit, D. Fichou, X. Peng and F. Garnier, “Thin-film transistors based on alpha-conjugated oligomers,” *Synthetic Metals,* Vols. 41-43, pp. 1127-1130, 1991.

[25] Z. Bao, A. J. Lovinger and A. Dodabalapur, “Organic field-effect transistors with high mobility based on copper phthalocyanine,” *Appl. Phys. Lett.,* vol. 69, pp. 3066-3068, 1996.

[26] M. Halik, H. Klauk, U. Zschieschang, G. Schmidt, S. Ponomarenko, S. Kirchmeyer and W. Weber, “Relationship Between Molecular Structure and Electrical Performance of Ogliophiophene Organic Thin Film Transistors,” *Adv.Mater,* vol. 15, p. 917, 2003.

[27] Y. Kawasugi, H. M. Yamamoto, M. Hosoda, N.Tajima, T. Fukunaga, K. Tsukagoshi and R. Kato, “Strain-induced superconductor/insulator transition and field effect in a thin single crystal of molecular conductor,” *Appl. Phys. Lett.,* vol. 92, no. 243508, 2008.

[28] H. Okamoto, S.Hamao, H. Goto, Y. Sakai, M. Izumi, S. Gohda, Y. Kubozono and R. Eguchi, “Transistor application of alkyl-substituted picene,” *Sci. Rep.,* vol. 10, no. 1038, 2014.

[29] N. Komura, H. Goto, X. He, H. Mitamura, R. Eguchi, Y. Kaji, H. Okamoto, Y. Sugawara and S. Gohda, “Characteristics of [6]phenacene thin film field-effect transistor,” *Appl. Phys. Lett.,* no. 101, p. 083301, 2012.

[30] R. Eguchi, X. He, S. Hamao, H. Goto, H. Okamoto, S. Gohda, K. Sato and Y. Kubozono, “Fabrication of high performance/highly functional field-effect transistor devices based on [6]phenacene thin films,” *Phys. Chem. Chem. Phys.,* no. 13, pp. 20611-20617, 2013.

[31] Y. Sugawara, K. Ogawa, H. Goto, S. Oikawa, K. Akaike, N. Komura, R. Eguchi, Y. Kaji, G. S. and Y. Kubozono, “O2-exposure and light-irradiation properties of picene thin film field-effect transistor: A new way toward O2 gas sensor,” *Sensors and Actuators B,* no. 171-172, pp. 544-549, 2012.

[32] X. He, R. Eguchi, H. Goto, E. Uesugi, S. Hamao, Y. Takabayashi and Y. Kubozono, “Fabrication of single crystal field-effect transistors with phenacene-type molecules and their excellent transistor characteristics,” *Org. Electron.,* no. 14, p. 1673–1682, 2013.

[33] X. He, S. Hamao, R. Eguchi, H. Goto, Y. Yoshida, G. Saito and Y. Kubozono, “Systematic control of hole-injection barrier height with electron acceptors in [7]phenacene single-crystal field-effect transistors,” *J. Phys. Chem. C,* no. 118, p. 5284–5293, 2014.

[34] H. Okamoto, R. Eguchi, S. Hamao, H. Goto, K. Gotoh, Y. Sakai, M. Izumi, Y. Takaguchi, S. Gohda and Y. Kubozono, “An extended phenacene-type molecule, [8]phenecene: synthesis and transistor application,” *Sci. Rep.,* no. 4, p. 5330, 2014.

[35] H. Okamoto, S. Hamao, H. Goto, Y. Sakai, M. Izumi, S. Gohda, Y. Kubozono and R. T. a. o. a.-s. p. Eguchi, “Transitor application of alkyl-substituted picene,” *Sci. Rep.,* no. 4, p. 5048, 2014.

[36] Y. Shimo, T. Mikami, H. T. Murakami, S. Hamao, H. Goto, H. Okamoto, S. Gohda, K. Sato, A. Cassinese and H. Y., “Transistors fabricated using the single crystals of [8]phenacene,” *J. Mater. Chem. C,* no. 3, pp. 7370-7378, 2015.

[37] Y. Shimo, T. Mikami, S. Hamao, H. Goto, H. Okamoto, R. Eguchi, S. Gohda, Y. Hayashi and Y. Kubozono, "Synthesis and transistor application of the extremely extended phenacene molecule, [9]phenacene," *Sci. Rep.,* no. 6, p. 21008, 2016.

[38] H. Okamoto, S. Hamao, R. Eguchi, H. Goto, Y. Takabayashi, P. Y.-H. Yen, L. U. Liang, C.-W. Chou, G. Hoffmann and S. Gohda, "Synthesis of the extended phenacene molecules, [10]phenacene and [11]phenacene, and their performance in a field-effect transistor," *Sci. Rep.,* no. 9, p. 4009, 2019.

[39] E. Pompei, C. Turchetti, S. Hamao, A. Miura, H. Goto, H. F. A. Okamoto, E. R. and Y. Kubozono, "Fabrication of flexible high-performance organic field-effect transistors using phenacene molecules and their application toward flexible CMOS inverters," *J. Mater. Chem. C,* no. 7, pp. 6022-6033, 2019.

[40] A. A. Ruzaiqi, H. Okamoto, Y. Kubozono, U. Zschieschang, H. Klauk, P. Baran and H. Gleskova, "Low-voltage organic thin-film transistors based on [n]phenacenes," *Org. Elctron.,* no. 73, pp. 286-291, 2019.

[41] A. Dodabalapur, J. Laquindanum, H. E. Katz and Z. Bao, "Complementary circuits with organic transistors," *Applied Physics Letters,* vol. 69, pp. 4227-4229, 1996.

[42] Y. Y. Lin, A. Dodabalapur, R. Sarpeshkar, Z. Bao, W. Li, K. Baldwin, V. R. Raju and H. E. Katz, "Organic complementary ring oscillators," *Applied Physics Letters,* vol. 74, pp. 2714-2716, 1999.

[43] B. K. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R.Sarpeshkar, H. E. Katz and W. Li, "Large-scale complementary integrated circuits based on organic transistors," *Nature,* vol. 403, pp. 521-523, 2000.

[44] B. K. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, J. H. O'Neil, R.Sarpeshkar, H. E. Katz and W. Li, "Design and fabrication of organic complementary circuits," *Journal of Applied Physics,* vol. 89, pp. 5125-5132, 2001.

[45] M. Lefenfeld, G. Blanchet and J. A. Rogers, "High-performance contacts in plastic transistors and logic gates that use printed electrodes of DNNSA-PANI doped with single-walled carbon nanotubes," *Advanced Materials,* vol. 15, pp. 1188-1191, 2003.

[46] D. J. Gundlach, K. P. Pernstich, G. Wilckens, M. Gruter, S. Haas and B. Batlogg, "High mobility *n*-channel organic thin-film transistors and complementary inverters," *Journal of Applied Physics,* vol. 98, pp. 064502/1-064502/8, 2005.

[47] Y. Inoue, Y. Sakamoto, T. Suzuki, M. Kobayashi and Y. Gao, "Organic thin-film transistors with high electron mobility based on perfluoropentacene," *Japanese Journal of Applied Physics,* vol. 44, pp. 3663-3668, 2005.

[48] B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski and T. J. Marks, "High-mobility bottom-contact *n*-channel organic transistors and their use in complementary ring oscillators," *Applied Physics Letters,* vol. 88, pp. 082104/1-082104/3, 2006.

[49] M.-H. Yoon, H. Yan, A. Facchetti and T. J. Marks, "Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics," *Journal of the American Chemical Society,* vol. 127, pp. 10388-10395, 2005.

[50] H. Klauk, U. Zschieschang, J. Pflaum and M. Halik, "Ultralow-power organic complementary circuits," *Nature,* vol. 445, pp. 745-748, 2007.

[51] K. Hizu, T. Sekitani, T. Someya and J. Otsuki, “Reduction in operation voltage of complementary organic thin-film transistor inverter circuits using double-gate structures,” *Applied Physics Letters,* vol. 90, pp. 93504-1, 2007.

[52] S. D. Vusser, S. Steudel, K. Myny, J. Genoe and P. Heremans, “Low voltage complementary organic inverters,” *Applied Physics Letters,* vol. 88, pp. 162116/1-162116/3, 2006.

[53] M. Kitamura and Y. Arakawa, “Low-voltage-operating complementary inverters with C60 and pentacene transistors on glass substrates,” *Applied Physics Letters,* vol. 91, pp. 053505/1-053505/3, 2007.

[54] A. Brown, C. Jarrett, D. d. Leeuw and M. Matters, “Field-effect transistors made from solution-processed organic semiconductors,” *Synthetic Metals,* vol. 88, pp. 37-55, 1997.

[55] H. Klauk, D. J. Gundlach and T. N. Jackson, “Fast Organic Thin-Film Transistor Circuits,” *IEEE ELECTRON DEVICE LETTERS,* vol. 20, no. 6, pp. 289-291, 1999.

[56] Y.-Y. Lin, A. Dodabalapur, R. Sarpeshkar, Z. Bao, W. Li, K. Baldwin, V. R. Raju and H. E. Katz, “Organic complementary ring oscillators,” *Appl. Phys. Lett.,* vol. 74, no. 18, p. 2714, 1999.

[57] L. Zhang, H. Wang, Y. Zhao, Y. Guo, W. Hu, G. Yu and Y. Liu, “Substrate-Free Ultra-Flexible Organic Field-Effect Transistors and Five-Stage Ring Oscillators,” *Adv. Mater.,* no. 25, pp. 5455-5460, 2013.

[58] B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski and T. J. Marks, “High-mobility bottom-contact *n*-channel organic transistors and their use in complementary ring oscillators,” *Appl. Phys. Lett,* vol. 88, p. 082104, 2006.

[59] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid and C. Dehm, “Flexible Organic Complementary Circuits,” *IEEE*

TRANSACTIONS ON ELECTRON DEVICES, vol. 52, no. 4, pp. 618-622, 2005.

[60] T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. M. Ramil, H. Sitter, M. Cölle and D. M. d. Leeuw, "High performance -channel organic field-effect transistors and ring oscillators based on C60 fullerene films," *Appl. Phys. Lett.,* vol. 89, p. 213504, 2006.

[61] D. M. Taylor, E. R. Patchett, A. Williams, Z. Ding, H. E. Assender, J. J. Morrison and S. G. Yeates, "Fabrication and simulation of organic transistors and functional circuits," *Chemical Physics,* vol. 456, pp. 85-92, 2015.

[62] H. Gold, A. Haase, A. Fian, C. Prietl, B. Striedinger, F. Zanella, N. Marjanovic´, R. Ferrini, J. Ring, K.-D. Lee, R. Jiawook, A. Drost, M. König, R. Müller, K. Myny, J. Genoe, U. Kleb, H. Hirshy, R. Prétôt, J. Kraxner, R. Schmied and B. Stadlober, "Self-aligned flexible organic thin-film transistors with gates patterned by nano-imprint lithography," *Organic Electronics,* vol. 22, pp. 140-146, 2015.

[63] Z. Ding, G. A. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett and D. M. Taylor, "Vacuum production of OTFTs by vapour jet deposition of dinaphtho[2,3-b:20,30-f]thieno[3,2-b]thiophene (DNTT) on a lauryl acrylate functionalised dielectric surface," *Organic Electronics,* vol. 31, pp. 90-97, 2016.

[64] K. Kuribara, Y. Hori, T. Katashita, K. Kakita, Y. Tanaka and M. Yoshida, "Organic physically unclonable function on flexible substrate operable at 2 V for IoT/IoE security applications," *Organic Electronics,* vol. 51, pp. 137-141, 2017.

[65] R. Eckstein, M. Alt, T. Rödlmeier, P. Scharfer, U. Lemmer and G. Hernandez-Sosa, "Digitally Printed Dewetting Patterns for Self-

Organized Microelectronics," *Adv. Mater.,* vol. 28, pp. 7708-7715, 2016.

[66] X. Zhang, T. Ge and J. S. Chang, "Fully-Additive Printed Electronics: Transistor model, process variation and fundamental circuit designs," *Organic Electronics,* vol. 26, pp. 371-379, 2015.

[67] M. Kondo, T. Uemura1, T. Matsumoto, T. Araki, S. Yoshimoto and T. Sekitani, "Ultraflexible and ultrathin polymeric gate insulator for 2V organic transistor circuits," *Applied Physics Express,* vol. 9, p. 061602, 2016.

[68] M. Li, D. K. Mangalore, J. Zhao, J. H. Carpenter, H. Yan, H. Ade, H. Yan, K. Müllen, P. W. Blom, W. Pisula, D. M. d. Leeuw and K. Asadi, "Integrated circuits based on conjugated polymer monolayer," *NATURE COMMUNICATIONS,* vol. 9, no. 451, 2018.

[69] E. Stucchi, G. Dell'Erba, P. Colpani, Y.-H. Kim and M. Caironi, "Low-Voltage, Printed, All-Polymer Integrated Circuits Employing a Low-Leakage and High-Yield Polymer Dielectric," *Adv. Electron. Mater.,* vol. 4, p. 1800340, 2018.

[70] H. Takahashi, M. Kitamura, Y. Hattori and Y. Kimura, "A ring oscillator consisting of pentacene thin-film transistors with controlled threshold voltages," *Japanese Journal of Applied Physics,* p. SBBJ04, 2019.

[71] C. P. Watson, B. A. Brown, J. Carter, J. Morgan and D. M. Taylor, "Organic Ring Oscillators with Sub-200 ns Stage Delay Based on a Solution-Processed p-type Semiconductor Blend," *Adv. Mater.,* vol. 2, p. 1500322, 2016.

[72] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong and T. Palacios, "Integrated Circuits Based on Bilayer

MoS2 Transistors," *American Chemical Society,* vol. 12, p. 4674−4680, 2012.

[73] J. Li1, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, H. Su and B. S. Ong, "A stable solution-processed polymer semiconductor with record high-mobility for printed transistors," *SCIENTIFIC REPORTS,* vol. 2, no. 754, 2012.

[74] Y. Kubozono, S. Hamo, T. Mikami, Y. Shimo, Y. Hayashi and H. Okamoto, "Transistor application and intercalation chemistry of pi-conjugated hydrocarbon molecules," *'Physics and Chemistry of Carbon-Based Materials: Basics and Applications,* no. 8, 2019.

[75] W. Salaneck, R. Friend and J. Brédas., "Electronic structure of conjugated polymers: Consequences of electron-lattice coupling," *Phys. Reports,* vol. 319, p. 231, 1999.

[76] G. R. Hutchison, Y.-J. Zhao, B. Delley, A. J. Freeman, M. A. Ratner and T. J. Marks, "Electronic structure of conducting polymers: Limitation of oligomer extrapolation approximations and effects of heteroatoms," *Phys. Rev. B,* vol. 68, p. 035204, 2003.

[77] W. Warta and N. Karl., "Hot holes in naphthalene: High electric-field-dependent mobilities," *Phys. Rev. B,* vol. 32, p. 1172, 1985.

[78] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Adv. Mater,* vol. 14, p. 99, 2002.

[79] D. Emin, "Correlated small-polaron hopping motion," *Phy. Rev. Lett.,* vol. 25, p. 1751, 1970.

[80] T. Holstein, "Studies of polaron motion," *Ann. Phys.,* vol. 8, p. 325, 1959.

[81] R. A. Street, J. E. Northrup and A. Salleo, "Transport in polycrystalline polymer thin-film transistors," *Phys. Rev.B,* vol. 71, p. 165202, 2005.

[82] G. Horowitz, “Organic field-effect transistors,” *Adv. Mater.,* vol. 10, p. 365, 1998.

[83] S. M. Sze and K. K. Ng, “Physics of Semiconductor Devices,” *Wiley Interscience,* 2007.

[84] T. Maeda, H. Kato and H. Kawakami, “Organic field-effect transistors with reduced contact resistance,” *Appl. Phys,,* vol. 89, p. 123508, 2006.

[85] T. Minari, T. Miyader, K. Tsukagoshi, Y. Aoyagi and H. Ito, “Charge injection process in organic field-effect transistors,” *Appl. Phys.,* vol. 91, p. 053508, 2007.

[86] J. Veres, S. Ogier and G. Lloyd, “Gate insulators in organic field-effect transistors,” *Chem. Mater.,* vol. 16, p. 4543, 2004.

[87] N. Benson, C. Melzer, R. Schmechel and H. v. Seggern, “Electronic states at the dielectric/semiconductor interface in organic field effect transistors,” *Phys. stat. sol. (a),* vol. 3, p. 475, 2008.

[88] C. A. Mills, D. M. Taylor, A. R. Jr. and A. P. Lee., “Effects of space charge at the conjugated polymer/electrode interface,” *J. Appl. Phys.,* vol. 91, p. 5182, 2002.

[89] R. H. Fowler and L. Nordheim, “Electron emission in intense electric fields,” *Proceedings of the Royal Society of London,* vol. 119, p. 173, 1928.

[90] S.-M. Kang and L. Y., CMOS digital integrated circuits, analysis and design, Boston: McGraw-Hill, 2003.

Acknowledgements

I want to thank all the people I met during my University career. In particular, I have to thank Prof. Claudio Turchetti for allowing me to complete my master thesis in collaboration with Prof. Yoshihiro Kubozono and his group at Okayama University. All of them played a fundamental role during my internship in Japan. Also, I greatly thank him for his support, valuable guidance and continuous encouragement and also for providing me the opportunity to work in a talented research team in Japan.

Two other people I have to thank are Prof. Luca Pierantoni and Prof. Bernard Chenevier for starting a collaboration between Universita' Politecnica delle Marche and Okayama University. Also, I'm in debt whit them for the occasion that they gave to me to talk about my research at Opto-X-Nano 2019 conference in Okayama. Another person that I met during my internship that I have to thank is Prof. Akihiko Fujiwara from Kwansei Gakuin University. He let me use his laboratory's equipment and deposit ZrO_2 gate dielectric on substrates. I want to express my gratitude to Ms. Shino Hamao, Ms. Noriko Kanemitsu, Dr. Ritsuko Euguchi and Prof. Hidenori Goto for their presence and advice during the lifetime at the laboratory.

Special thanks go to my friends Niccolò Di Basilio, Carlo Capretta, Alessio Tarquini, Lorenzo Abbadini, Paolo Compagnoni e Nicholas Di Pierdomenico and the people who know me and believed in me encouraging me with their words and presence. Also, I want to thank them for the great time spent with me during my free time.

Last but not least, I also would like to thank my family very much for their love, their patience and for sustaining me all this time.