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Corso di Laurea in Ingegneria Elettronica

Design a PA for satellites communications

Progettazione di un PA per applicazioni satellitari

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Acknowledgments

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Ancona, Dicembre 2023

Giovanni Di Pietrantonio

Abstract

The objective of this thesis is to investigate radiation effects, specifically Single Event Transients (SETs), on RF circuits and to develop an effective modelling approach to observe the output effects in various power amplifier topologies. This work investigates the radiation hardness of SETs in three different amplifier topologies: cascaded, pseudo-differential common emitter, and differential common emitter. The amplifiers operated within a frequency band of 17-22 GHz and met the design specifications. The layout of the best-performing amplifier will be implemented.

Sommario

Lo scopo di questa tesi è studiare gli effetti di radiazione, in particolare i SET (Single Event Transient), sui circuiti RF e trovare un buon modo per modellarli al fine di osservare gli effetti sull'uscita in diverse topologie di PA. In questo lavoro, i SET sono stati osservati in un amplificatore a cascata, in un emettitore comune pseudo-differenziale (emettitore comune senza sorgente di corrente all'emettitore) e in un emettitore comune differenziale (emettitore comune con sorgente di corrente), al fine di osservare quale delle tre topologie esibiva una maggiore durezza di radiazione. Tutti questi amplificatori lavoravano in una banda compresa tra 17 GHz e 22 GHz e dovevano soddisfare le specifiche di progetto. Successivamente, verrà realizzato il layout dell'amplificatore risultato migliore.

Contents

Chapter 1

Radiation effects in microelectronics

The main purpose of this thesis was to analyse SETs, one of the effects of space radiation. At the circuit level, SETs are modelled by current injection (using an ideal current source) at the target node of the circuit. Two concepts are widely used: macro modelling, where the current source is implemented between the target node and ground, and micro modelling, where the source is implemented within the target transistor.

Before discussing this specific effect in more detail, the following is a general discussion of the main radioactive effects in space[1].

1.1 Cumulative effects

These are long-term effects that can cause changes in the characteristics of devices and circuits, resulting in malfunctions and ultimately functional failure. Cumulative effects include:

- **TID (Total Ionizing Dose)**: this effect is induced by the ionizing energy from radiation exposure and produces the creation of electron-hole pairs in the component material. These charges typically are trapped in the dielectric layer or in the bulk of the dielectric or at or near the dielectric interface whit the semiconductor where the electric effect on the device operation is maximum. TID produces a variety of effects on the circuits. TID is expressed in Gray (Gy) or rad (100 rad = 1 Gy), with 1 Gy = 1 J/kg.

- **TNDI (Total Non-Ionizing Dose)**: also called DD (Displacement Damage). This effect is caused by the transfer of energy through non-ionising means, specifically through the interaction of primary and secondary energetic particles with component atoms. This interaction can create damage and stable electrically active defects in the semiconductor crystal lattice. This can cause a variety of effects in bipolar devices and all types of optoelectronics, including CCD and APS detectors, LED and laser diodes. It is worth noting that typically ASICs and FPGAs are not affected by TNID.

1.2 Single Event Effects (SEEs)

There are a lot of different type of SEEs but is possible to group them in two macro categories: non-destructive and destructive SEE. There are a lot of different type for each one but the more important for this work are SETs. A SET (Single Event Transient) is a non-destructive SEE and is a temporary excursion at a node in an integrated circuit (it visible as a voltage spike). It is generated by particle ionizing the semiconductor and passing through or near a sensitive junction, in worst case it can degenerate in a SEU or SEFI. When SET happens in an analog circuit it is called ASET (Analog SET), in case of a digital circuit DSET (Digital SET). In the follow a description of the other type of SEEs.

1.2.1 Non-destructive SEEs

- **SEU (Single Event Upset)**: A SEU is a single bit flip, meaning a change in the state of a storage element. SEUs can be silent if unused or corrected by error correction code (ECC), or they can cause various effects at the circuit level, including circuit malfunction or SEFI. The sensitivity to SEUs greatly varies depending on the technology, design, and electrical operation. Small transistor dimensions and reduced supply voltage can decrease the critical charge, which is the minimum charge collected at a sensitive node that can induce a state change. This can increase sensitivity to SEEs.

- **MCU(Multiple-Cell Upset) and MBU(Multiple-Bit Upset)**: A MCU refers to the change of state of two or more logic cells caused by a single particle strike. The corrupted cells are not always physically adjacent. The MBU is a specific case of MCU that occurs when corrupted cells are located within the same word. It cannot be corrected by a simple error correction code. As technology scales, the gaps between transistors in integrated circuits become smaller, making them more susceptible to multiple upsets. When an energetic particle deposits charge, it can affect several sensitive nodes, resulting in single-event upsets (SEUs) in multiple memory cells.

- **SEFI(Single Event Functional Interrupt)**: tSEFI is a type of soft error that can cause a component to malfunction, reset, or lock up. This type of error is commonly found in complex devices that have built-in state and control sections, such as modern memories like SDRAM, DRAM, NOR-Flash, and NAND-Flash. There are two main types of SEFI: those that require a reset by software and those that require a reset by power cycling. It is important to note that SEFI can result in the loss of stored data.

1.2.2 Destructive SEEs

- **SEL(Single Event Latch-up)**: It is a phenomenon that can occur in CMOS circuits when a parasitic thyristor (PNPN or NPNP structures) is triggered [2]. This can result in a high current flow that, if the power supply is maintained, can lead to the destruction of the device due to thermal effects. The SEL signature is a self-sustaining current that flows in the low impedance path of the triggered parasitic thyristor structure, and its gain increases with temperature. The only way to remove SEL is to power-reset the circuit. SEL should not be confused with temporary current spikes caused by SET-induced logic conflicts or SEFI.

- **SESB(Single Event Snap-Back)**: Another type of potentially destructive single event effect, similar to SEL with a self-sustaining current signature but less common, is the single event snap-back (SESB). The SESB is caused by the triggering of a parasitic bipolar structure (NPN or PNP). For instance, when each transistor is dielectrically isolated from its neighbours, silicon-on-insulator (SOI) MOS is not sensitive to SEL, but it can be sensitive to SESB due to floating body effects when body contacts are insufficient.

- **SEHE(Single Event Hard Error)**: A SEHE, also known as a 'stuck bit', is an unalterable change of state resulting from permanent or semi-permanent damage to a cell caused by an ion strike. This type of error is commonly encountered in all types of memories and digital devices.

- **SEB(Single event Burnout)**: SEB refers to the triggering of the parasitic bipolar structure in a power transistor, typically n-channel, accompanied by regenerative feedback, avalanche, and high current conditions. It is potentially destructive unless suitably protected. SEB is not frequent in Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs), except in the case of embedded lateral or vertical power devices.

- **SEGR(Single Event Gate Ruptere) or SEDR(Single Event DIelectric Rupture)**: SEGR or SEDR is the destructive rupture of a gate oxide or any dielectric layer caused by a single ion strike. This results in leakage currents under bias and can be observed in power MOSFETs, linear integrated circuits (with internal capacitors), or as stuck bits in digital devices. There is no effective protection against Single Event Gate Rupture (SEGR) or Single Event Dielectric Rupture (SEDR) caused by energetic heavy ions in dielectrics. This is due to the extremely fast energy transfer and damage, which occurs in less than a picosecond, compared to the response time of any electrical protection such as filtering.

The table below summarises the main effects of a single event commonly found in various types of technologies and families of components.

Technology	Family	Function	SEL, SESB	SEGR, SEDR	SEB	SEU	MCU/MBU	SEHE	SEFI	SET
			destructive SEE			Non-destructive SEE				
Power MOS				X	X					
CMOS, BiCMOS and SOI	Digital	SRAM	X			X	X	X		
		DRAM	X			X	X	X	X	
		FPGA	X			X	X	X	X	X
		Flash EEPROM	X			X		X	X	
		µP / µcontroller	X			X	X		X	X
	Mixed signal	ADC	X	X	X	X			X	X
		DAC	X	X	X	X			X	X
	Linear		X	X	X					X
Bipolar	Digital			X	X	X				X
	Linear			X	X	X				X

Figure 1.1: Summary of SEEs. In this table is shown which SEEs are of interest for each specific application.

Chapter 2

What is and how to characterize a SET

To begin, it is important to understand the behaviour of ions when they come into contact with a pn-junction. Figure 2.1 [3] illustrates the effects of ion particles.

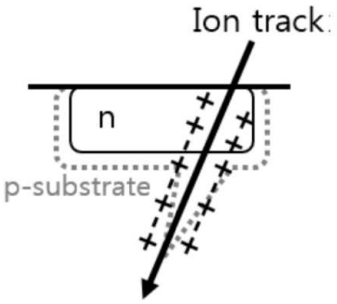

Figure 2.1: Each heavy ion particle produces an ionization track.

Figure 2.1 shows that a high-energy particle triggers a single-event effect (SEE) when it enters an electronic device, creating electron-hole pairs (EHP) along the ion track. The node potential changes as these electrons switch, which can trigger a single-event upset (SEU) in a digital circuit.

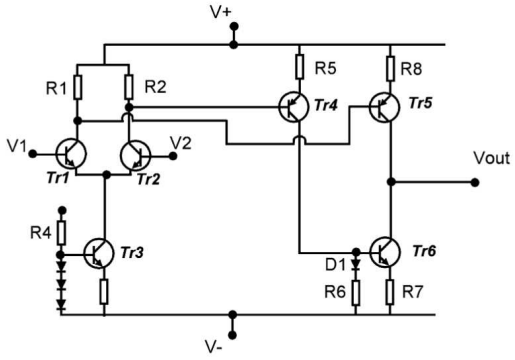

Figure 2.2: Circuit elements for a simple operational amplifier with six transistors [**?**]. For the example, to see what would happen to the voltage output if an ion were to strike Tr1.

In [4] an example is shown to explain how SETs propagate to V_{out} in the circuit in

Figure 2.2. Charge injected into the C/B junction of Tr1 will cause the E/B junction to be slightly more forward biased. As a result I_1 will increase and I_2 will decrease. An increase in I_1 will increase the voltage drop across R_1 and a decrease in I_2 will decrease the voltage drop across R_2. Both voltage transients will propagate through the operational amplifier, the positive transient to the base of transistor Tr4 and the negative transient to the base of Tr5. Tr5 becomes more conductive and Tr6 becomes less conductive. Together they cause the output voltage to fall. When the excess change stored in transistor Tr1 disappears, the voltage drop across R_1 and R_2 returns to its original value and so does the voltage at the base of Tr5 and Tr6. V_{out} gradually recover and the SET effect disappears.

This section clarifies how ions change the polarization of a junction when they strike it. The following section will discuss how to model this behaviour at the circuit level. At this level, SETs are modelled by a current injection (with an ideal current source) at the target node of the circuit when ions strike it. There are two concepts widely used [5]:

- Macro modeling: the current source is implemented between the target node and ground.
- Micro modeling: in this case the source is implemented whit in the target transistor.

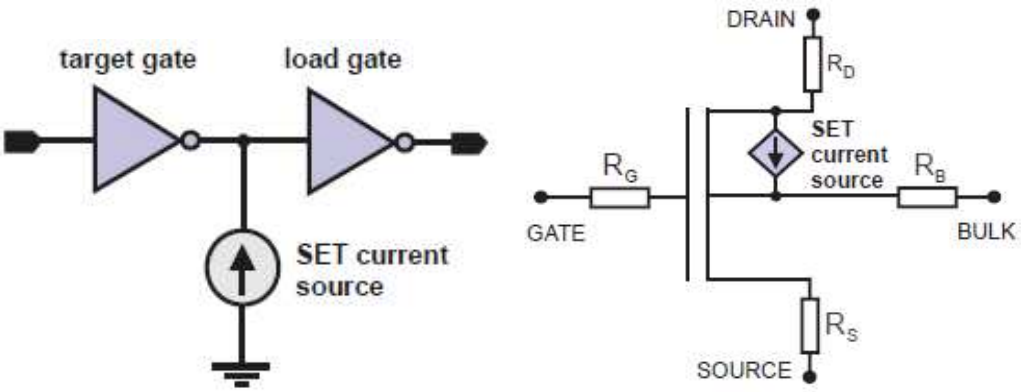

Figure 2.3: In this figure, (a) show how to apply a SET in case of macro-model, instead, (b) show the SET in micro-model

Macro-modelling is easy to implement, which is why it is the most popular. On the other hand, micro-modelling requires modification of the transistor model as it needs to be integrated into the target transistor. Therefore, the micro-modelling concept can only be applied for SET simulation when the transistor models are available. Beyond this, numerous models for the SET-induced current have been proposed, and they can be classified into six major groups.:

1. Models based on single voltage-independent current sources: The model is inaccurate because it does not consider the dependence between induced current and node voltage.

2. Models based on voltage-dependent current source: Implementing this model is challenging and requires extensive calibration.

3. Models based on two voltage-independent current source: As the first one.

4. Models based on piecewise interpolation: Calibrating this model requires circuit or device simulation.

5. Model based on look-up table: Calibrating this model requires device simulations or experiments.

6. An alternative approach to the current injection model (1)-(5) employs a switch ans a series resistor to reproduce the SET response.

The existing modeling and simulation approaches have both advantages and disadvantages. For an in-depth analysis of these aspects, please refer to [5]. The purpose of this work is to create a circuit from scratch, which means that only models with ideal current sources (1) and (5) can be used.

2.1 Models based on single voltage independent current source

The typical implementation of this model involves a macro model that connects a current source between the ground terminal and the target node (as shown in Figure 2.3(a)), however, as demonstrated in (cite) and (cite), a bipolar transistor also utilises a current source between the pn-junctions of the device. As explained in the second quote, calibration is necessary to set the amplitude and duration of the pulse when applying the current source in this manner. A mathematical model for the current source is required as a starting point for calibration.

Below is a brief overview of various mathematical models that can be used depending on the circuit's purpose.

2.1.1 Double exponential current model

This is the most widely used model for simulating the SET-induced current:

$$I_{SET(t)} = \frac{Q_{coll}}{\tau_f - \tau_r}(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}})$$

The Q_{coll} denotes the charge collected, τ_r is the collection time of the junction or the rise time of the curve and τ_f is the ion-track establishment time constant or the fall time. The parameters τ_r and τ_f depends from the technology and are related

between them but there is not a surely correct relate for these parameters (this is discussed in section 2.2).

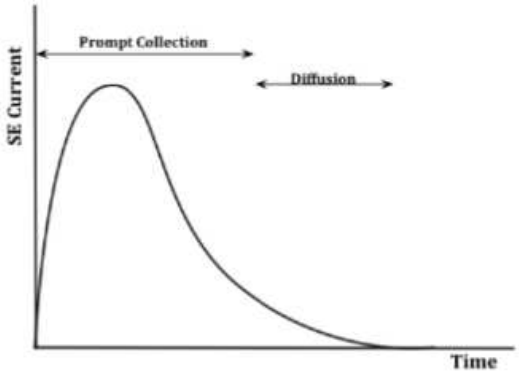

Figure 2.4: Shape of pulse make with double exponential current model

2.1.2 Freeman's current model

This model has been used for estimating the critical charge of bipolar memory cell, but it can also be utilized for characterization of other logic block. This model has the advantage than it use a single parameter τ (dependent always from the technology)

$$I_{SET}(t) = \frac{2}{\sqrt{\pi}} \frac{Q_{coll}}{\tau} \sqrt{\frac{t}{\tau}} e^{\frac{-t}{\tau}}$$

2.1.3 Hu's current model

This is the only model that consider impact of the angle incidence ϕ, however, for use this model is necessarily required the knowledge of the depletion layer width W.

$$I_{SET}(t) = \frac{I_0}{\cosh^2\left(\frac{I_0 t \cos\phi}{2.5\times10^{-10}W}\right)}$$

2.1.4 Diffusion current model

This model define SET current in term of I_{max} (the peak of SET current pulse) and t_{max} (the time to reach the max amplitude of the current pulse). This mode is useful for long SET which result from the diffusion collection process.

$$I_{SET}(t) = I_{max}(e^{t_{max}/t})^{3/2}(e^{-3t_{max}/2t})$$

2.1.5 Roche's Current model

This is a very simple model because it only need two parameters: I_0, the current amplitude, and t, the decay time constant.

$$I_{SET}(t) = I_0 \cdot e^{-t}$$

2.1.6 Rectangular current model

This model is defined only by two parameter: the amplitude I_{AMP} and the duration of the pulse T. Usually whit this model the rise time and the fall time of the rectangle are considered 0 but it's possible to include a small piece of time for rise and fall time. In any case this model ignore the most important physical effects of SET so it can only be use when the physical aspect are not cared. If we consider no rise and fall time the model is:

$$I_{SET}(t) = \begin{cases} I_{SET} & \tau_1 < t < \tau_2 \\ 0 & \tau_1 > t > \tau_2 \end{cases}$$

2.1.7 Triangular current model

[h] This model is simplified of the double exponential current model, in this case is only require the value of the peak of current I_{max} and the rise time τ_r, the fall time is calculate by one of the relations in section 2.2 (usually in this case is used $\tau f = 40 \cdot \tau_r$ because the SET has a long tail in the shape of its pulse). It is implemented like a piecewise function).

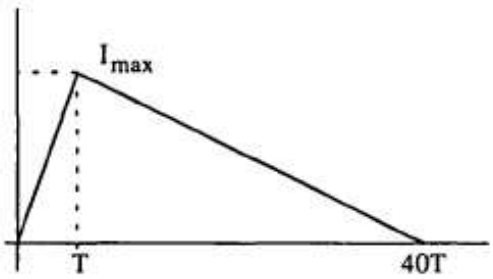

Figure 2.5: Shape of a triangular model current pulse

2.2 Current amplitude and time duration of a SET

Defining the model is not the only problem in characterizing a SET but, as mensioned above it is necessary to define how large and how long (in term of time) it is. These parameters were observed in CMOS technology, and most of the simulations were performed using CMOS. Therefore, the literature only allows for comparison of these parameter values within this technology. Comparing several papers ([**?**] and [6]), it seems that realistic amplitude values range from a few tens of μA to even about $450\mu A$, since the duration of the pulse would be of the order of $1ns$.

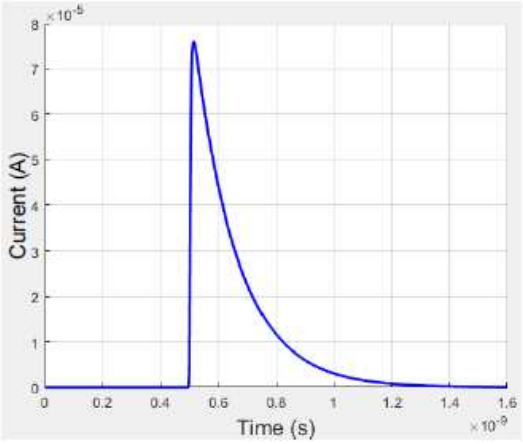

Figure 2.6: transient current pulse generated in the drain of an N-type off-transistor due to a particle strike in that region, as function of time[7]

Given this, the question is how to relate the rise time τ_r to the fall time τ_f. Various methods of doing so will be explained in the following chapter.

To enable comparison of simulation results, it is crucial to express the current through the collected charge, Q_coll. This charge penetrates the inside of the transistor and causes the recombination of the electron-hole pair. Alternatively, the Linear Energy Transfer (LET) can also be used to express the current. LET represents the average energy dispersed per unit length when a particle passes through a material. At this point, it is important to highlight the difference between Q_coll and critical charge Q_crit. Q_coll was defined earlier, whereas Q_crit represents the minimum charge value at which a bit-flip occurs, also known as the threshold value for a Single-Event Upset (SEU). The concept of critical charge can also be applied to linear circuits. However, the value of Q_crit for linear devices is somewhat arbitrary since it must be related to a measurable quantity, such as ASET amplitude. Therefore, any definition of Q_crit should include the criterion used for measuring it. Q_crit can be defined as the minimum amount of charge required to produce a given amplitude ASET in a particular operating configuration. The term may also refer to a system application that requires a minimum charge to be collected in order to modify the system. Experiments have shown that the LET thresholds for some linear bipolar devices are very small, on the order of $1MeV\acute{L}cm^2/mg$, which is equivalent to a depositing $0.01pC$ per micron [8]. Such a low LET begs the question as to whether the cause is small Q_{crit} and a small collection depth or a large Q_{crit} and a large collection depth. Experiments ([9] , [4])have shown that the Q_{crit} is approximately $1pC$ on the tested devices, indicating a considerable depth of penetration. The charge penetrated up to $100\mu m$, according to the results cited.

According to experimental results, a Q_{coll} is considered heavy, which is the worst case, when it reaches $2pC$ (large ion case) and light when it reaches a few hundred fC (small ion case).

Chapter 3

SET simulations

3.1 Model SETs

I could not find any simulations of SET in bipolar transistors in the literature. Therefore, it appears that there are no reliable methods to simulate this effect using this type of transistor. This work employed an ideal current source to simulate ion injection, as demonstrated in [4] in Chapter V. However, the specific model to be used was not specified, so the double exponential model was chosen due to its widespread use. Figure 3.1 illustrates the connection of ideal current sources between the transistor junctions. The reason for multiplying the current pulse by the number of fingers ('f' in the figure) will be explained shortly. In the simulations, the ideal generators are activated one at a time, not simultaneously.

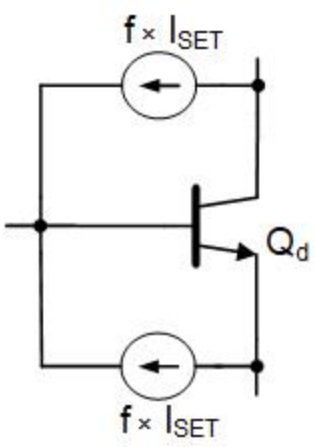

Figure 3.1: Transistor BJT whit SET generators, the 'f' is the transistor number of fingers

Each I_{SET} is multiplied for the number of transistor fingers because the double exponential model mimics an ion striking the junction from above, but this doesn't represent the worst case as it occurs when all the fingers in the transistor are struck by the ion (see Figure 3.2).

Having decided which mathematical model to use and with which methodology to use it, the problem now is how to obtain the shape of the pulse shown in Figure 2.4 in

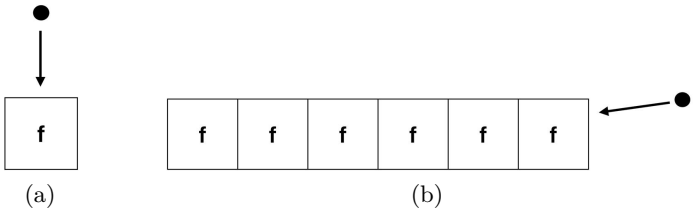

Figure 3.2: In (a) is showed how the double exponential model work, a ion strike from the top only one finger, but in a bigger transistor, for example a transistor with 6 fingers like in (b), the worst case is when the ion strike all the fingers, for this reason to simulate this the I_{SET} is multiplied for the number of fingers

term of magnitude and time duration. In order to give a value to the variables Q_{coll}, τ_r and τ_f in the I_{SET} expression, I proceeded by trial and error until I obtained a result that was consistent with the duration, magnitude and value of the charge collected as discussed above. Two examples, one with a heavy ion and one with a light ion, are shown in Figure 3.3.

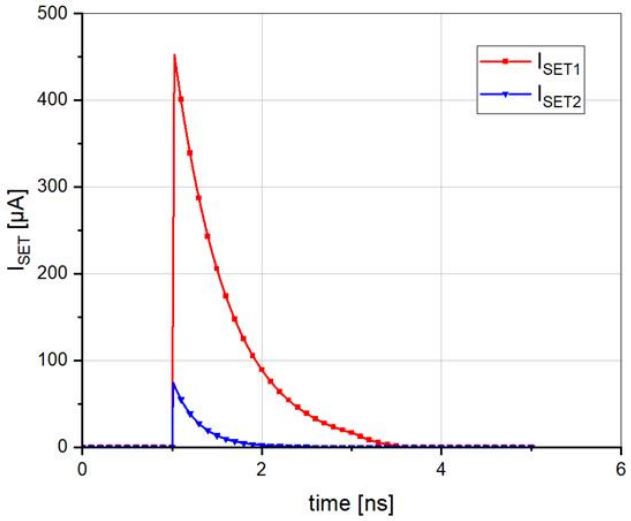

Figure 3.3: The bigger and smaller simulated SET pulses. The big one (the red one) have $Q_{coll} \approx 0.96pC$ and $\tau_r \approx 12ps$, the smaller (the blue one) have $Q_{coll} \approx 1.44pC$ and $\tau_r \approx 25ps$.

Regarding the two time variables τ_f and τ_r, as with the mathematical model, there is no reliable value to give them. However, they are related and there are different proportions that can be used between them:

- $\tau_f = 4 \times \tau_r$
- $\tau_f = 4.6 \times \tau_r$
- $\tau_f = 24 \times \tau_r$

- $\tau_f = 39 \times \tau_r$

As stated in the literature, there is no clear preference between the two options. However, as mentioned in [5], the first two options are widely used and there is a formula, dependent on the technology, to obtain one of the two variables:

$$\tau_f = \frac{k\epsilon_0\epsilon_r}{q\mu N_D}$$

However, for this work, I utilized the third option to obtain the desired outcome.

3.2 SET in three different topologies

During my thesis work, I designed and tested three different amplifier topologies for satellite communication in the 17-22GHz band. The goal was to determine which topology had the best radiation-hardened properties. The three topologies were cascode, differential common emitter (a common emitter with a current source at the emitter), and pseudo-differential common emitter (without the current source, the emitter is connected to the ground). All simulations have been conducted using a differential structure because, as explained in chapter 8 of the reference [1], this design choice helps to mitigate the effects of single-event transients (SETs). To ensure a fair comparison and comply with project specifications, all amplifiers were designed with similar characteristics in terms of S-parameters, gain, OP1dB, and OIP3. It's worth mentioning that during the simulations, it was observed that gain has a negative effect on the SET effect. Specifically, the circuit with higher gain (but a different coupling network) exhibited a longer signal distortion duration.

To apply a SET in an amplifier, only one SET generator should be turned on at a time. It is sufficient to use these generators in just one of the two branches in the differential amplifiers, either in the positive or negative branch. This is because the differential output does not change if the SET is applied in one or the other branch, as long as the generator is the same in the same transistor in the other branch. Additionally, it has been observed in simulations that the SET's effect is the same whether the base-emitter or the base-collector generator is turned on in one transistor.

Below is a summary of the simulations carried out for each topology. All amplifiers had a gain of approximately 16dB within the band, an OP1dB of 13dBm at the center of the band, and both S_{11} and S_{22} were less than -10dB across the entire band. Additionally, the OIP3 was at least 26dBm within the band.

3.2.1 SETs in cascode

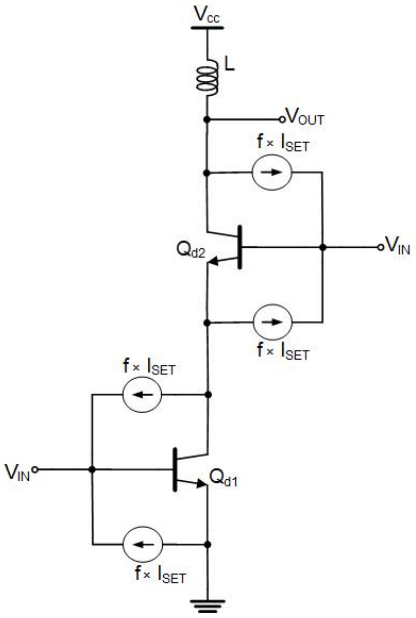

Figure 3.4: An example of a single-ended cascode with SET generators

To meet the previously specified parameters, a single stage was sufficient. The transistor in this amplifier had 16 fingers. To make a complete comparison, two different bias circuits were used: one with a voltage divider using resistors and the other with a voltage divider using diodes. In the latter case, SET generators were also added to the bias circuit. SET pulses were simulated using all generators with varying magnitudes. One of the worst cases is shown below.

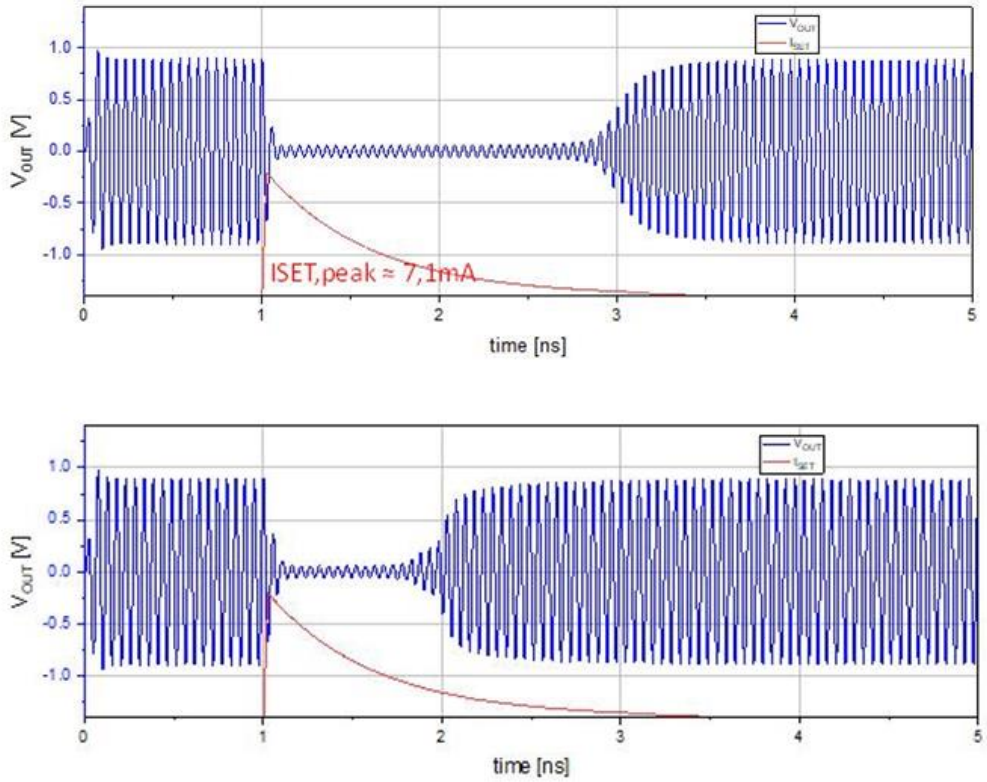

Figure 3.5: The result at top is obtained when a voltage divider whit resistor are used, the one at the bottom is with divider with diodes. This specific case is when to be turned on is the SET generator between the base-collector junction

It has been observed that when a bias circuit is used with a resistor voltage divider, the SET effect lasts longer compared to the case with diodes that recover the voltage output 1ns earlier.

3.2.2 SETs in differential common emitter

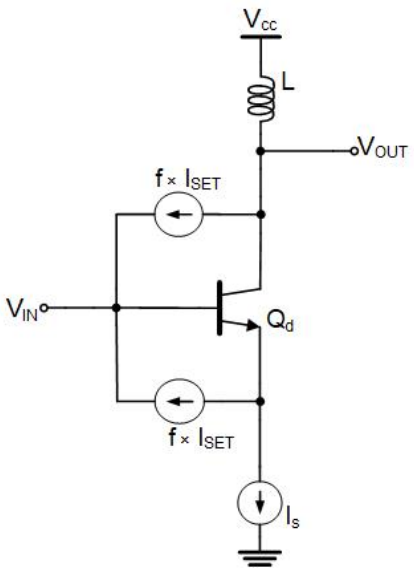

Figure 3.6: An example of a single-ended differential common emitter with SET generators

To meet the project parameters, an amplifier with two stages was constructed. The first stage had 18 fingers, while the second stage had 32 fingers. Two different bias circuits were used to observe any potential behavioral differences, similar to the cascode configuration. Furthermore, the current source (I_S) in this case was created using a current mirror consisting of two BJTs. Additionally, SET generators were implemented on these transistors.

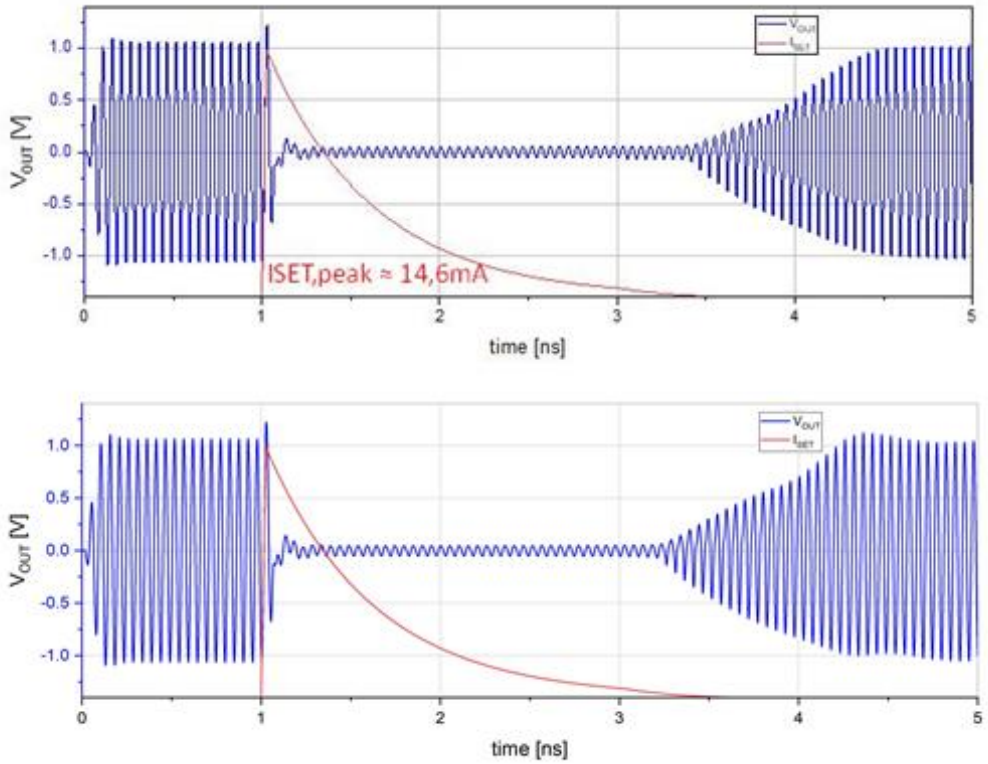

Figure 3.7: The result at top is obtained when a voltage divider whit resistor are used, the one at the bottom is with divider with diodes. This specific case is when to be turned on is the SET generator between the base-collector junction

A slight improvement was observed with the diodes bias, however, the results were still deemed unacceptable as the signal took a long time to recover from the SET application. Figure 3.7 shows the results obtained with the SET applied in the second stage. Regarding SETs in the mirror, no changes have been observed in the voltage output.

3.2.3 SETs in pseudo differential common emitter

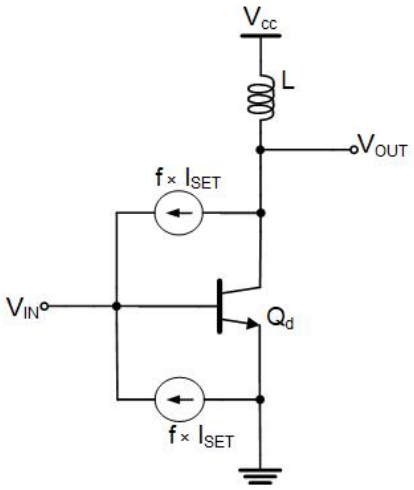

Figure 3.8: An example of a single-ended pseudo differential common emitter with SET generators

This configuration is the same as the differential common emitter, the only difference being the presence of the current source in the emitter (I_s in Figure 3.6, which is absent here).

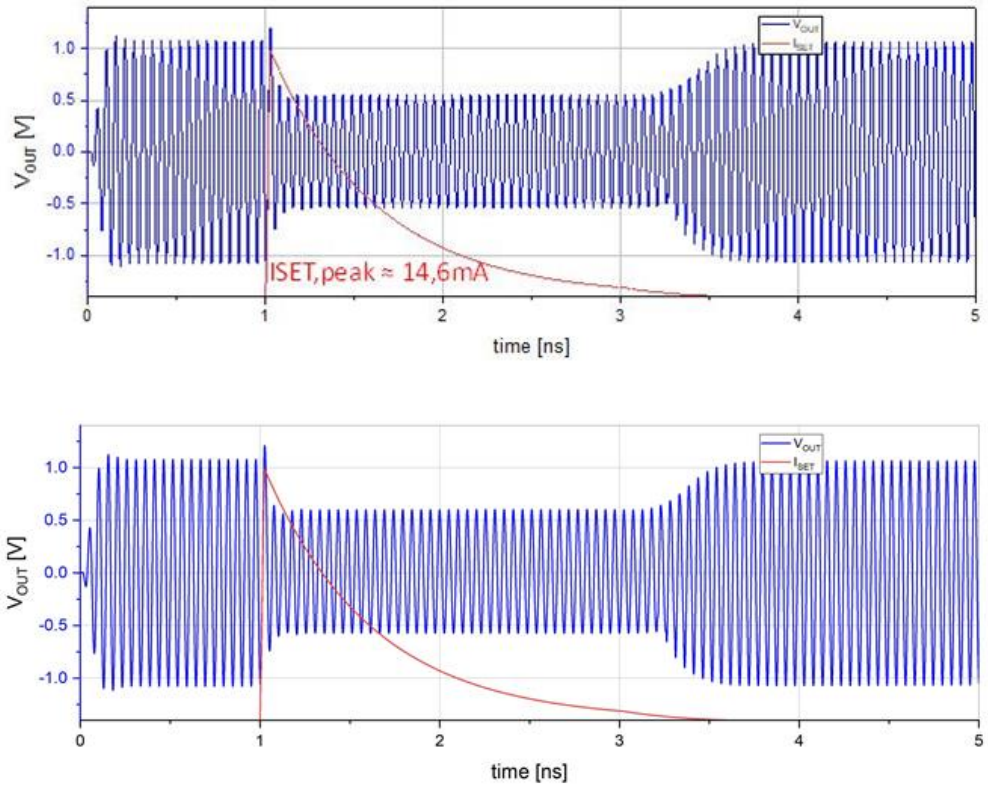

Figure 3.9: The result at top is obtained when a voltage divider whit resistor are used, the one at the bottom is with divider with diodes. This specific case is when to be turned on is the SET generator between the base-collector junction

As before the figure shows one of the worst cases, as in the previous common emitter the SET has been used in the second stage. As in all previous topologies, there is a slight improvement when the diodes are biased, but the situation is still better than with the differential common emitter.

3.2.4 Bias circuit

As shown in the previous section, changing the bias circuit from a resistive divider to a diode divider can improve the voltage output, in some cases, as shown in the following figure, the difference is very obvious.

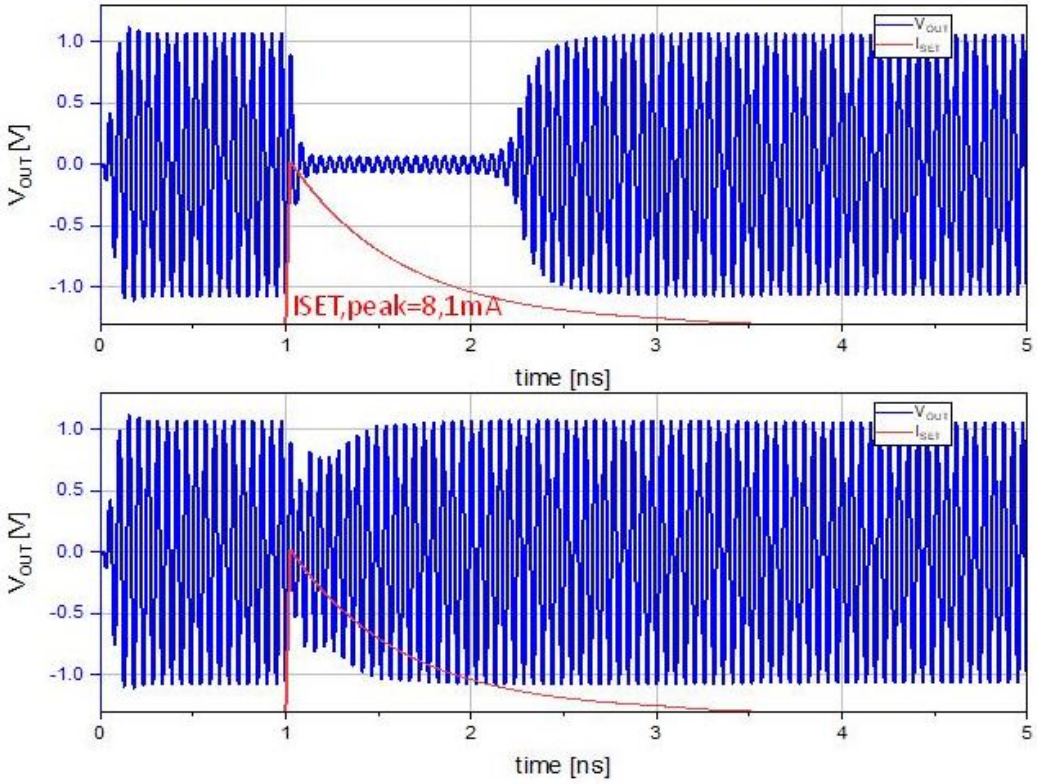

Figure 3.10: How the differential voltage output change with the bias circuit. In this case is turned on the SET generator in the first stage of pseudo differential common emitter (a very similar result is obtained also in the differential common emitter). At the top is showed the output when the voltage divider with resistor is used, in the bottom the divider with diodes

This Figure 3.10 is for a SET occurring in the first stage of the pseudo differential common emitter, as can be seen the effect is almost zero. However, in the diode

polarization there are pn junctions, so the SET generator should also be inserted between them, as it can also occur here. Fortunately, the simulations don't show any distortion of the output voltage when one of the SET generators is turned on in these bias circuits, this is true for all three topologies.

Chapter 4

Circuit layout

The results of the schematic simulations indicate that the pseudo differential common emitter is more radiation-hardened than the other two options. For this reason, we chose and implemented the layout of such a topology.

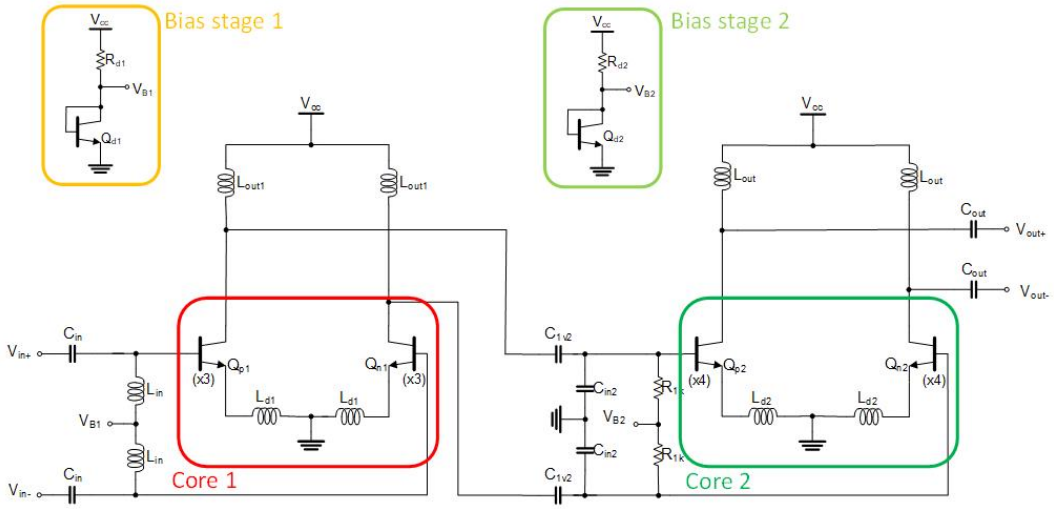

Figure 4.1: The chosen circuit. Have been highlighted the two stage cores and the bias circuits.

Cadence Virtuoso was used to create the layout. The final layout, shown in Figure 4.2, has dimensions of 1 x 0.9 mm^2. The different parts of the layout will be observed in the following sections.

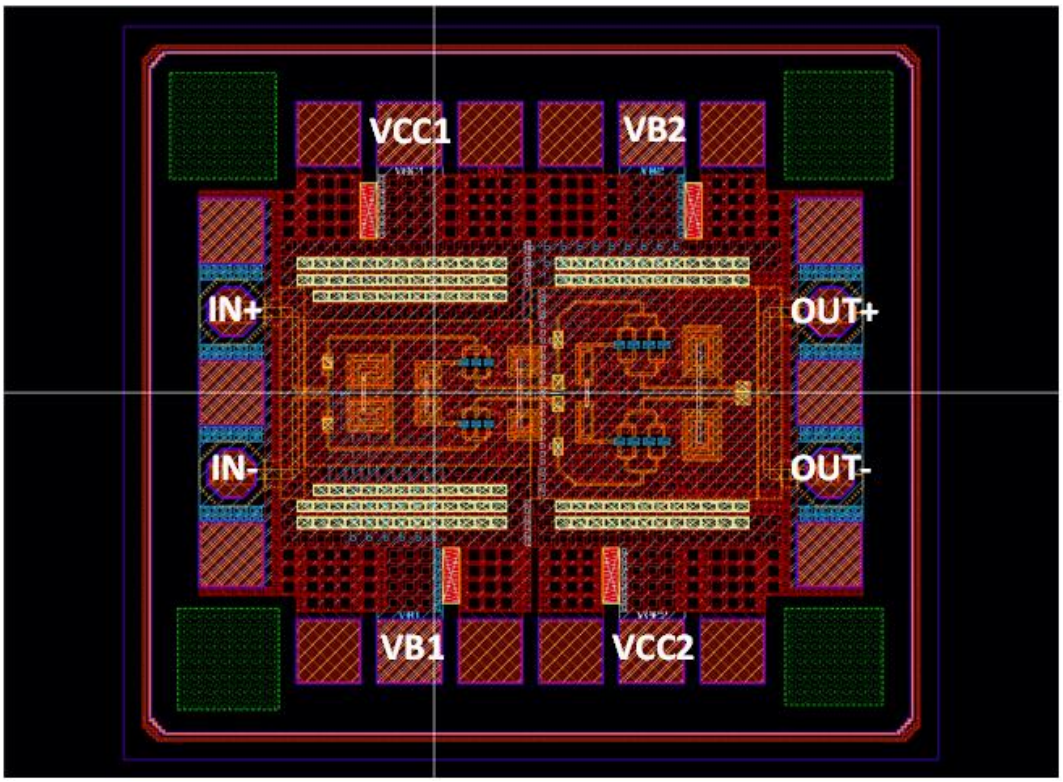

Figure 4.2: Final layout

4.1 Layout without grid

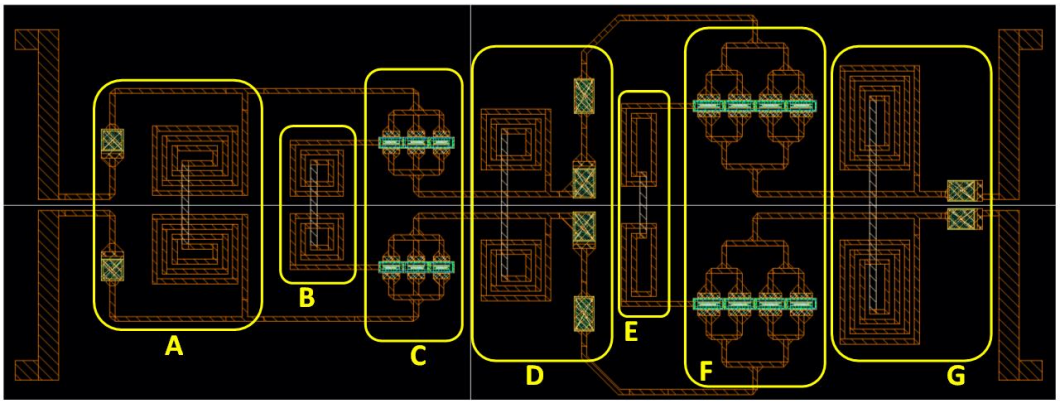

Figure 4.3: In this figure has been divided the circuit in its parts and identified with a letter

The initial section of the layout illustrates the cores. The first core (C) comprises three transistors, each with six fingers, totalling 18 fingers. The second core (F), on the other hand, consists of four transistors, each with eight fingers, totalling 32 fingers. The lines were set at 3 µm. Both cores underwent simulation in ADS (Advanced Design System) and were subsequently integrated into the schematic to verify their proper functionality. The design process began with the creation of the

inductive degenerations and coupling network. The degenerations, B for the first core and D for the second, were integrated into the scheme after EM simulation to ensure core stability. The next step is to create the matching networks A, D and G. They are made one at a time, starting with the input matching network A. The lines from the transistor bases, the inductance and the capacitance are EM-simulated separately first because, as a single block, they would require a lot of time to be simulated. Some variations to the single components previously mentioned were carried out in order to improve the results. Once all the individual components had been simulated, they were simulated as a single block to give a more accurate EM model.The procedure was repeated for both the output adaptation network (G) and the adaptation network between the two stages (D). The design of the latter was made as compact as possible to minimize the occupied surface. On both sides in figure 4.3, before the input net and forward the output net there are four lines (not highlighted). These lines connect the circuit to the necessary pads for measuring the circuit.

Since the circuit is all EM simulated, I simulated it with SET generators and the voltage output was the same in the simulations as in the schematic for each SET generator turned on. After simulating the entire circuit using EM simulation, the SET generators were repositioned at the junctions as indicated in chapter 3. The voltage output matched the schematic for each activated SET generator, both in schematic simulation with ideal component and in simulation with EM modeled components.

After creating the circuit shown in Figure 4.3, the input and output pads were added (as seen in Figure 4.2: IN+, IN-, OUT+, and OUT-), along with polarisation pads (VCC1, VB1, VCC2, VB2) and metal grids. Additionally, several decoupling (or bypass) capacitors were placed along the top and bottom of the circuit to prevent any potential interference between channels. The non-highlighted pads are intended for grounding. Between a ground pad and a bias pad, there is a MOSFET (the ones in bright red) used to prevent discharges.

The following graphs display the S-parameters, OIP3, and centre-band gain (with an arrow indicating OP1dB), while the final results are summarised in the table below.

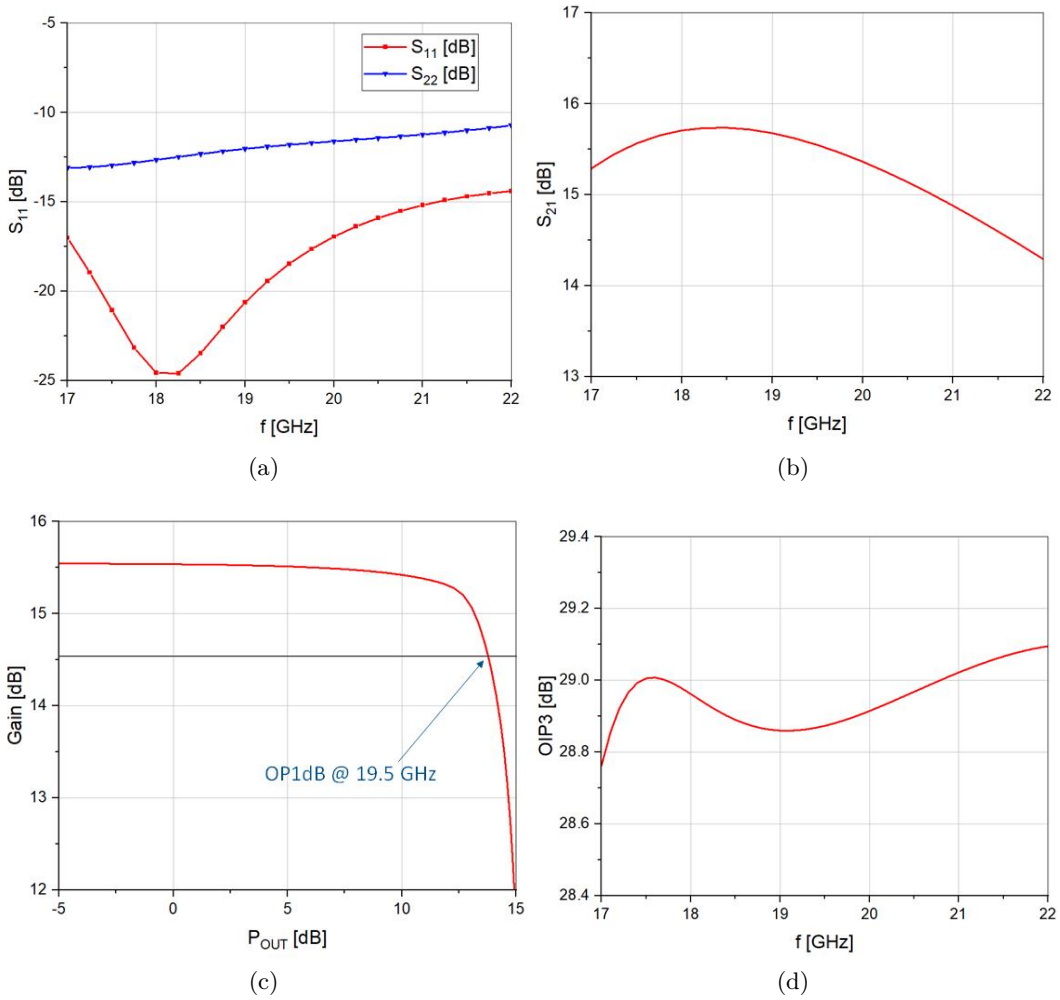

Figure 4.4: (a)Parameters S_{11} and S_{22} (b) S_{21} (c)Gain (d)OIP3

Parameter	Simulated	Comments
BW [GHz]	15 - 24	3 dB BW
OIP3 [dBm]	>28.8	In band
OP1dB [dBm]	13.65	@ 19.5 GHz
PAE [%]	15.8	@ OP1dB
PAE [%]	11.7	@ 3dB backoff
S_{21} [dB]	15.73	Peak @ 18.5 GHz
S_{11} [dB]	<-14.4	In band
S_{22} [dB]	<-10.7	In band
NF [dB]	<4	In band
In band ripple [dB]	1.4	—
P_{DC} $[mW]$	78.4 @ 1.65 V	2.75 mW on bias branches

Chapter 5

Conclusions

Based on the simulations, it appears that the common differential emitter is the least effective topology, likely due to the current source on the emitter being seen as an opening. Simulations using voltage divider diodes indicate that the SET effect has a shorter duration with polarization, as demonstrated in Figure 3.10. Therefore, it can be concluded that the pseudo-differential common emitter with voltage divider diode in polarization is the most suitable topology for a radiation-resistant PA. Additionally, it seems that the amplifier gain has a negative impact on the destructive effect of the SET. Specifically, a higher gain results in a longer and more significant destructive effect. However, further analysis is required to confirm this.

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